REMARKS

I. 35 USC 112-1 REJECTIONS

1.1 Reasons Of Record

The Applicant respectfully traverses the 35 USC 112-1 rejections (the "112-1" rejections) for the reasons of record and for the additional reasons discussed herein.

The disclosure rejections fail to establish a non-prima facia case for the reasons of record and for the reasons set forth below.

1.2 The Instant Disclosure Provides The Epitome Of A "Self-Contained Embodiment"

The instant disclosure provides the epitome of a "self-contained embodiment" (discussed below). This despite the fact that the Appellant cannot find any law and the Examiner did not cite to any law that requires such a "self-contained embodiment". Thus, the disclosure goes further than the law requires in providing an adequate disclosure.

The claims are directed to a system having novel combinations of features. Various embodiments of the system are disclosed in a "top-down" and "end-to-end" format. The application discloses an entire system (e.g., Figs. 1A and 6A) in extensive detail (e.g., Figs. 6B-6AH). However, the Examiner does not properly consider the disclosure and in particular the disclosure as set forth in Fig. 1A (an end-to-end disclosure). Thus, the following is submitted as a rebuttal to the Examiner's remarks.

The system is disclosed in great detail both in the figures and in the description, where the description describes the figures in great detail down to the component and the sub-component levels of detail. The top-down and end-to-end format

includes details from the front-end to the back-end and from the block diagram level of detail down to the electronic component, pin, and wire level of detail and even down to the sub-component level of detail.

The top-down format ranges from a more general top level shown in block diagram form down to a very detailed level of schematic diagrams with actual commercially available IC components and actual wire interconnections between numbered pins on the IC components. The details do not stop there, but continue down to the sub-component level of detail. The sub-component details include the schematic diagrams and design details of the IC components that are incorporated-by-reference from the Motorola Schottky TTL Data book and include the design details of the computer, disk drives, display monitor, printers, and other devices that are incorporated-by-reference from the design manuals.

The end-to-end format ranges from input circuits at the front-end to output circuits at the back-end and includes in detail the in between software and circuits (such as the processors, memories, and digital filters).

The top-down format of the instant disclosure is consistent with the guidance provided by the Federal Circuit.

> DeGeorge not only disclosed the TCCPI circuit in block diagram format in the '670 application but also disclosed it in detailed schematic format within the same disclosure, together with an extensive verbal description....
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> We conclude that the enablement requirement of §112 was satisfied by disclosure of detailed, *claimed* TCCPI circuitry without requiring detailed disclosure of all related, *unclaimed* circuitry with which the TCCPI might be interfaced.

DeGeorge.[6] Similarly, the Applicant "not only disclosed the [inventions] in block diagram format ... but also disclosed it in

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6. DeGeorge v. Bernier, 768 F.2d 1318, 226 USPQ 758, 762-763 (Fed. Cir. 1985).

detailed schematic format within the same disclosure, together with an extensive verbal [written] description ...."

A system block diagram is shown in Figs 1A and 1P with various blocks that are shown in greater detail in other figures. For example, many of the blocks shown in Fig. 1A are expanded to provide greater detail in Figs. 1C-1G and in the "Modular Configuration Features Table" (Spec. at 24-30). Effectively, the more detailed block diagrams in Figs. 1C-1G are intended to fit within the corresponding blocks in Fig. 1A and the more detailed functions in the "Modular Configuration Features Table" are intended to fit within the corresponding blocks in Fig. 1A (Spec. at 5, 17, 17; respectively (emphasis added):

> ... where **Fig 1A** is a block diagram representation of one configuration of the system of the present invention; Fig 1B is a block diagram of a geometric module configuration; **Fig 1C** is a block diagram of a single channel configuration of one configuration of the present invention **in accordance with a reduced implementation of Fig 1A**; **Fig 1D** is a block diagram of a geometric processor module **in accordance with Fig 1A**; **Fig 1E** is a block diagram of a spatial processor module **in accordance with Fig 1A**; **Fig 1F** is a block diagram of input sources, input interfaces, and input multiplexers/demultiplexers **in accordance with Fig 1A**; Fig 1G is a block diagram of an output interface, output multiplexers/demultiplexers, and output devices **in accordance with Fig 1A**; ....
>
> The block diagram shown in **Fig 1A** illustrates the modular expandability of the system of the present invention, **shown in greater detail in Figs 1B to 1G**.
>
> One general purpose modular configuration is shown in **Figs 1A to 1G** and **summarized in the MODULAR CONFIGURATION FEATURES TABLE herein**.

Furthermore, regarding Fig. 1P, an input device 115A is shown in block diagram form in Fig. 1P and is shown in very detailed schematic form in Figs. 6U-6V, an address generator 115B is shown in block diagram form in Fig. 1P and is shown in very detailed schematic form in Figs. 6O-6R, a memory 115C is shown in block diagram form in Fig. 1P and is shown in very detailed schematic form in Figs. 6E-6N, a buffer 115D is shown in block diagram form in Fig. 1P and is shown in very detailed schematic

form in Figs. 6X-6AF, and an output device 115E is shown in block diagram form in Fig. 1P and is shown in very detailed schematic form in Figs. 6S and 6T.

Furthermore, Fig. 6A illustrates another block diagram with various blocks that are shown in greater detail in other figures. For example, control logic 610B shown in block diagram form in Fig. 6A is shown in very detailed schematic form in Figs. 6B-6D, address generators 610C are shown in block diagram form in Fig. 6A and are shown in very detailed schematic form in Figs. 6O-6R, memory 610D is shown in block diagram form in Fig. 6A and is shown in very detailed schematic form in Figs. 6E-6N, and buffer 610E is shown in block diagram form in Fig. 6A and is shown in very detailed schematic form in Figs. 6X-6AF.

Intermediate level figures are provided to further disclose the invention. For example, Fig. 2M provides intermediate level detail[7] to further illustrate the address generator block 115B and the memory block 115C (Figs. 1P and 2M). Other figures (e.g., Fig. 5A, 5D, 6A, and 6E) also provide various intermediate levels of detail.

The figures are described in detail in the extensive disclosure comprising **over 600 pages** of description and figures. The sections of the specification and the figures are functionally grouped together. For example, the section entitled Address Generators (Spec. at 319-328) discusses the detailed schematic diagrams related to the address generator figures (Figs. 6O-6R). The disclosure is outlined with the Table of Contents.

The level of detail is illustrated by the disclosure of an "Experimental System" that was **actually** reduced-to-practice (e.g., Spec. at 240-373 and 544-574 and Figs. 6A-6AH and 7D), including highly detailed schematic diagrams down to the individual component and individual wire level of detail (See,

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7. Fig. 2M is intermediate between the block diagram of an address generator 115B and a memory 115C in Fig. 1P and the detailed schematics of an address generator in Figs. 6O-6R and a memory in Figs. 6E-6N.

e.g., Figs. 6B-6D), detailed descriptions thereof down to the individual component and individual wire level of detail (See, e.g., Spec. at 240-373), cable wire lists (See, e.g., Spec. at 503-521), IC component (DIP) location on circuit boards (See, e.g., Spec. at 522-543), and actual Basic[8] program listings with instructions and detailed annotations (See, e.g., Spec. at 544-574).

The Table of Contents provides a top-down road map (an **indented** outline) of the sections in the disclosure. Top-tier sections include:

GRAPHICS PROCESSOR
SPATIAL FILTERING
MEMORY ARCHITECTURE
BUFFER MEMORY
EXPERIMENTAL SYSTEM

middle-tier sections for the top-tier EXPERIMENTAL SYSTEM section include:

EXPERIMENTAL SYSTEM ARCHITECTURE[9]
LOGIC BOARD
MEMORY BOARDS
BUFFER BOARD
REAR-END BOARD
CIRCUIT SPECIFICATIONS

and lower-tier sections for the middle-tier EXPERIMENTAL SYSTEM ARCHITECTURE section include:

General Description[10]
Supervisory Processor Interface
Image Loading
Software
Description of DIS.ASC Listing

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8. "Basic" is a higher level computer language, available in both a compiler and an interpreter.

9. This is the second indented tier in the Table of Contents.

10. This is the third indented tier in the Table of Contents.

Circuit Boards
Cable List
S-100 Bus System

The section in the specification entitled Brief Description of the Drawings (Spec. at 5-14) provides another type of top-down list of the disclosure. For example, Fig. 6A is identified as "a block diagram" and Fig. 6B is identified as "a detailed schematic diagram" (Spec. at 7).

In addition, extremely detailed tables of cabling and component placement (Spec. at 503-543) and computer source programs (Spec. at 544-574) are disclosed.

The "Experimental System" is an actual reduction-to-practice system that was actually constructed; including, for example, the computer, the computer programs, the computer interface, the address generators, the image memory, the buffer memory, the weight circuitry, the kernel circuitry, and the display monitor. For example, the instant application discloses a computer (e.g., Spec. at 155-60, 241-99, and 575-76 and element 610A in Fig. 6A) filtering an image with a disclosed filter program (e.g., Spec. at 161-180 and 561-566 and Fig. 7D), overlaying graphics vectors into image memory with a disclosed program and initializing address generators and displaying an image with a disclosed program (e.g., Spec. at 155-60 and 544-60). The instant application also discloses an image memory (e.g., Spec. at 181-218 and 329-36, element 115C in Figs. 1P and 2M, element 610D in Fig. 6A, and Figs. 6E-6N) storing image information and being accessed by the address generators (e.g., Spec. at 319-28 and 115B in Figs. 1P and 2M, Figs. 4A and 4B, element 610C in Fig. 6A, and Figs. 6O-6R); a buffer memory (e.g., Spec. at 219-39 and 337-65 and element 115D in Fig. 1P, element 610E in Fig 6A, and Figs. 6W-6AF) buffering accessed image information; a weight circuit generating kernel weights (e.g., Spec. at 161-80, 363-65, and 561-66 and Figs. 5A, 5D, and 6AH), a kernel circuit generating a kernel of image information (e.g., Spec. at 161-80, 360-62, and 561-66 and Figs. 5A-5D and 6AG); a display interface

(e.g., Spec. at 366-71 and element 520 in Fig. 5A and Figs. 6S-6T) generating display information; and a display monitor (e.g., Spec. at 366-71, element 115E in Fig. 1P, output from element 610E in Fig. 6A, and Figs. 6S-6T) displaying an image. All of these disclosures and more are compatible and are **combined** in the "Experimental System".

The "Experimental System" further implements an input arrangement (e.g., joysticks, Spec. at 366-71, element 115A in Fig. 1P, and Figs. 6U-6V).

The "Experimental System" further implements an output arrangement (e.g., a display monitor with a video interface, Spec. at 366-71, element 115E in Fig. 1P, output from element 610E in Fig. 6A, and Figs. 6S-6T).

The "Experimental System" further implements a block memory with a detailed disclosure of a block having eight rows, eight columns, and 64 samples or pixels; an accessing or reading circuit; and a writing circuit (e.g., Spec. at 181-218 and 329-36, element 115C in Figs. 1P and 2M, element 610D in Fig. 6A, and Figs. 6E-6N).

The "Experimental System" further implements memory address generators (e.g., Spec. at 319-28 and 115B in Figs. 1P and 2M, Figs. 4A and 4B, element 610C in Fig. 6A, and Figs. 6O-6R).

The "Experimental System" further implements a computer with detailed disclosures of computer programs (e.g., Spec. at 155-60, 241-47, and 544-74, 610A in Fig. 6A, and Fig. 7D).

The "Experimental System" further implements a spatial processor and a filter processor (e.g., Spec. at 161-80 and 561-66 and Fig. 7D).

The "Experimental System" further implements a graphic processor generating vector information (e.g., Spec. at 155-60, 544-60, and 567-574).

The "Experimental System" further implements a kernel circuit including a kernel memory and a kernel processor (e.g., Spec. at 161-80, 360-65, and 561-66; and Figs. 5A-5D, 6AG, and 7D).

The "Experimental System" further implements a weight arrangement (e.g., Spec. at 161-80, 363-71, and 562 and Figs. 5A, 5D, 6AH, and 7D).

1.3 The Fact That The Appellant Reduced-To-Practice An "Experimental System" Is Very Significant To § 112-1

The Appellant actually reduced-to-practice and disclosed in detail an "Experimental System". This is very important to § 112-1. However, the Examiner misrepresents the disclosure of this "Experimental System". Hence, for this reason alone, the § 112-1 rejections fail to establish a prima facie case.

The Appellant even produced video tapes to the PTO under the Disclosure Document program, incorporated these video tapes by reference into the instant application, and discussed these video tapes and the demonstrations recorded thereon in the instant specification (Spec. at 146-150). However, the Examiner disregarded these video tapes.

According to the Deputy Assistant Commissioner for Patent Policy and Projects,[11] such a reduction-to-practice is particularly relevant to the issue of § 112-1.

> If a specification demonstrates actual reduction to practice by showing that the inventor constructed an embodiment or performed a process that met all the limitations of the claim and determined that the invention would work for its intended purpose, one skilled in the art would clearly recognize that the applicant was in possession of the claimed invention.

The Assistant Commissioner cites to Cooper[12] for an authority.

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11. Stephen G. Kunin, "Written Description Guidelines and Utility Guidelines," Journal of the Patent and Trademark Office Society (JPTOS), Vol. 82, No. 2 at page 86 (February 2000).

12. Cooper v. Goldfarb, 154 F.3d 1321, 1327, 47 USPQ2d 1896, 1901 (Fed. Cir. 1998).

In view of the above, the Examiner has ignored this very important evidence and hence, for this reason alone, the § 112-1 rejections should be reversed.

1.4 The Wands Analysis

The Examiner alleges a Wands analysis but instead wanders off into irrelevant issues and makes self-serving conclusory statements. In effect; the Examiner fails to focus on the eight factors, instead making erroneous and conclusory statements regarding lack of disclosure. The Examiner fails to establish the required findings of fact supported by the required "substantial evidence" or conclusions of law supported by proper authorities. Hence, the contention of undue experimentation is not properly supported and thus the § 112-1 enablement rejection should be reversed.

Further, although the original claims as a whole are not recited verbatim in the instant claims, the recitations in the original claims are still relevant to the written description rejection. See also the discussion of the original claims in Section 1.5.7 herein.

The eight factors are addressed in the MPEP at 2164.01(a) through 2164.08. See also Wands.[13] The Examiner lists the Wands factors but his lengthy discussion related thereto continues to assert only conclusory and irrelevant statements. Because the Examiner does not provide proper evidence, much less the required "substantial evidence", these Wands factors establish that there is **no** undue experimentation.

a. The breadth of the claims: The instant application has a range of breadth of claims. The Examiner has selected a broad "example" claim which is more easily enabled than narrower

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13. In re Wands, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed, Cir. 1988).

claims. See MPEP 2164.08 ("the only relevant concern should be whether the scope of enablement provided ... is commensurate with the scope of protection sought by the claims."). See also Moore.[14]

b. The nature of the invention: the Examiner's selected "example" claim is directed to a computer system.

c. The state of the prior art: the state of the relevant arts was high, as established in Sections 1.7 and 1.14.3 - 1.14.5 herein. For example, by 1984, the Appellant was able to purchase a computer; a display monitor; a TV display chip that provided the necessary synchronization, blanking, interlace, and other signals to control the display monitor. See the MM5321 integrated circuit chip in Fig. 6T and in the Spec. at 366-367 and much more. See the disclosed actually reduced-to-practice "Experimental System".

d. The level of one of ordinary skill: is consistent with the statement in item c. above.

e. The level of predictability in the art: the level of predictability of the relevant arts was high, as established in Sections 1.7 and 1.14.3 - 1.14.5 herein. This predictability was significantly enhanced by the design, construction, testing, and disclosure of the actually reduced-to-practice "Experimental System".

f. The amount of direction provided by the inventor: the inventor disclosed in detail an actually reduced-to-practice "Experimental System" and other disclosures in the format of a top-down end-to-end disclosure. See also the Table of Contents

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14. In re Moore, 439 F.2d 1232, 1236, 169 USPQ 236, 239 (CCPA 1971).

(Section 1.2 herein) the Brief Description Of The Drawings (Spec. at 5-9).

g. The existence of working examples: the inventor disclosed in detail an actually reduced-to-practice "Experimental System" and other disclosures.

h. The quantity of experimentation needed to make or use the invention based upon the content of the disclosure: the inventor disclosed in detail an actually reduced-to-practice "Experimental System" and other disclosures. See the law on the absence of experimentation for a computer program type invention in Sections 1.14.3 - 1.14.5 herein. And a computer patent disclosure need only teach "the functions of the software" (Section 1.7 herein).

1.5 The Examiner Misrepresents The Issue Of Interconnections and Interrelations

1.5.1 The Examiner Disregards The Computer Programming Nature Of Claim Limitations When Complaining About Interconnections And Interrelations

The Examiner objects to the disclosure of "interconnections and interrelations" without explaining what abstract concept he has in mind. The Examiner is certainly not representing that a computer, or a memory, or a computer program has a problem with "interconnections and interrelations". Programs are sequences of computer instructions, computers and memories were well known in the art, commercially available computer and memory products were used in the disclosure, and memories are disclosed in detailed schematic and textual form with numerous interconnections. And a computer patent disclosure need only teach "the functions of the software" (Section 1.7 herein).

As an example, a commercially available computer and commercially available computer memories were used in the disclosed actually reduced-to-practice "Experimental System" and documentation on these commercially available products were filed in the PTO in the Disclosure Document program and incorporated-by-reference into the instant application (Spec. at 575-576).

Even more compelling, the extensively disclosed computer in the actually reduced-to-practice "Experimental System" was not properly considered by the Examiner. This is most likely the reason why the Examiner cannot find the disclosed interconnections and interrelations, the Examiner disregarded the disclosed interconnections and interrelations.

As a further example, a program is coded in sequence and the computer executes it in sequence. Thus, adjacencies between instructions constitute "interconnections and interrelations" and the progression of program execution by the computer. Computer programs also contain non-sequential instructions; branch instructions, jump instructions, subroutine call instructions, return from subroutine instructions, and the like. These non-sequential instructions are well defined in the art. Branch instructions, jump instructions, and subroutine call instructions identify the destination by address, mnemonic, or the like embedded in the instruction. Return instructions return to the program location from which they came. Such computer instructions were well known since the 1960s and before.

The Examiner misrepresented the significant computer program related disclosures in the instant application. The **original** Summary of the Invention identifies "software" improvements in the instant application and has significant software-related disclosures: (Spec. at 4 (heading emphasis in original, all other emphasis added)):

> SUMMARY OF THE INVENTION
>
> The present invention is generally directed to improved processing systems and, in particular, provides improvements in memory, processor, **software**, and control architectures and in **software** and hardware designs. A

system architecture is provided that provides flexibility, performance, and efficiency. A geometric processor is provided that implements rotation, translation, expansion, compression, warping, 3D-perspective, vector generation, and other features in a high performance and efficient manner; such as by using a window implementation and by providing the flexibility of **software** control. A spatial processor is provided that provides smoothing, anti-aliasing, and other features. Memory architectures and designs are provided that increase performance and efficiency, including a memory map and a buffer memory. **Programs** are provided that enhance flexibility and capability, yet preserve the high performance of the hardware. For example, efficient geometric initial condition generation and time domain interpolation enhance performance. Many other novel and valuable features are disclosed.

In view of the above, it is not clear why the Examiner would even bring up "interconnections and interrelations" in this programming environment. He uses the term indiscriminately and without explaining its meaning or relevance. It is not reasonable in view of the computer software nature of claim limitations.

1.5.2 The Disclosure Has Verbatim And Near-Verbatim Disclosure Of Interconnections and Interrelations

The disclosure has verbatim and near-verbatim disclosure of claim limitations. Many of the interconnections are recited as being between two claim limitations that are disclosed verbatim or near-verbatim. For example, the single "Overlays" section of the disclosure teaches interconnections and interrelations, many of which are actual "working examples" of the interconnections and interrelations. Many of the interconnections and interrelations are recited as being between two claim limitations that are disclosed verbatim or near-verbatim and that are shown in the figures as being interconnected.

Further, navigational and sensor elements are taught operating in this same "Overlays" section in conjunction (Spec. at 387):

> Overlays can include pictorial features, annotation symbols, imaginary pathways for map displays, and other such overlays. In a military application; overlays can be related to fire control, bombing, sensors, and navigation. Navigation information can include GPS, inertial, celestial, radar, Tercom, dead-reckoning, and other navigation information. Sensor information can include radar, infra-red, video, sonar, and other sensor information.

The software embodiment provides interconnections and interrelations through the software. However, the Examiner has not adequately articulated his rejection, nor provided the required "substantial evidence", nor established the required prima facie case; but merely makes generalized erroneous conclusory statements about interconnections and interrelations.

The Examiner does not clarify whether he is seeking hardwired interconnections, program interconnections, or what; only that he cannot find any interconnections or interrelations. However, the Examiner has totally ignored the "working examples" of the computer loading and overlaying of the image information into the image memory, such as with the LD.ASC computer program and with the "Image Loading" computer operations (Spec. at 246). A computer loading image information into an image memory and the computer overlaying image information onto the image information stored in the image memory is significant interconnections and interrelations.

Regarding the software "interconnections and interrelations", the Examiner has apparently disregarded the fact that computer programs are expressly "interconnected and interrelated" and that computers, computer memories, and programs stored in the memories and executed in the computers are expressly "interconnected and interrelated".

Regarding the hardware "interconnections and interrelations", the Examiner has not properly considered the detailed block diagrams and schematic diagrams and the detailed descriptions thereof in the disclosure.

In the actually reduced-to-practice "Experimental System" the image memory is the interface between the computer and the display and the various image-related claim limitations are taught in the disclosure as being loaded into image memory. Pictorial images are loaded as discussed in the section entitled "Image Loading" (Spec. at 246) and the generated images (e.g., graphic images) are generated and overlaid with the LD.ASC program (Spec. at 155-160 and 547-560). Thus, it is not clear what interconnections and interrelations the Examiner is complaining about. The claimed interconnections and interrelations are disclosed with "working examples".

In addition to the above, implementing the claims with the disclosed computer software embodiment makes express the interconnections and interrelations between the computer program instructions (Section 1.5.1 herein).

1.5.3 The Examiner's Erroneous Conclusory Statements Regarding Unidentified Interconnections And Interrelations Are Wrong As A Matter Of Fact And As A Matter Of CCPA Law

The Examiner's erroneous conclusory statements regarding interconnections and interrelations are wrong as a matter of fact and as a matter of CCPA law. The facts establish that the interconnections and interrelations are disclosed in great detail. The law establishes that disclosure of interconnections and interrelations are not necessary when there is no apparent reason why the combination would not be operable and when an artisan would understand the interconnection or interrelation.

Despite the fact that the instant disclosure provides extensive relevant interconnections and interrelations and combinations, including both hardware and software

interconnections and interrelations and combinations, **such a disclosure is not necessary**. The CCPA established that disclosure of the functions that an artisan might reasonably combine **is sufficient** in the absence of an apparent reason "why a substitution ... would not be operable". See Byrne.[15]

> Recalling appellants' explicit statement that the jet turbine of Figure 1 may be substituted for the rewind motor shown in Figure 2, it is apparent that the only material respect in which the embodiment of Figure 2 resulting from that modification fails to support count 4 is in the use of friction brakes instead of fluid brakes for the reel. The board found as a fact that appellants' "description does not *explicitly* state anywhere that the water brake of the embodiment shown in Figs. 12 and 13 may be substituted for the friction brakes * * * in the combinations as shown in any of the other figures of the drawing." (Emphasis ours). While such finding is undeniably correct, **we think the board's position puts entirely too restricted an interpretation on the language of the application**, and particularly on the aforementioned reference to figures 13 and 14 as illustrating an embodiment "in which we employ the principles of a water brake for the same purposes as set forth and described heretofore with respect to the embodiments of Figures 2 and 7." **No reason being apparent why a substitution of the water brake would not be operable, we think this statement constitutes a clear and unequivocal disclosure of that substitution to a person of ordinary skill [1] in the art.** The issue is not, as might be inferred from the board's opinion, whether one following appellants' specification would necessarily "produce" or select the particular combination of the counts for his own use. **Rather, it is whether he would necessarily recognize that such a combination was *disclosed* as a construction which might be selected if desired**. The present application clearly discloses an alternative construction embodying the combination of count 4. Consequently, it supports that count and also the less limited combinations of counts 3 and 5.

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15. Byrne v. Trifillis, 442 F.2d 1390, 170 USPQ 32, 34 (CCPA 1971) (emphasis added).

The Board in Nelson followed the law articulated in Byrne:[16]

> Bowler argues ... that there is no specific teaching in Nelson to modify Example 5 to obtain the compounds of the counts. Thus, Bowler urges that although Nelson discloses in the list of substituents the required meta substituents of the counts, Nelson also disclosed the ortho and para substituents, among others, and there is no indication of preference for the substituents of the counts and therefore there is no reason to single out the required meta substituents. **In our view, however, the issue is not** whether one following the Nelson disclosure would necessarily produce the compounds or prefer the particular disclosed substituents (m-chloro or m-trifluoromethyl) required to prepare the compounds of the counts; rather, **it is whether he would necessarily recognize that such a combination was disclosed as a construction which might be selected if desired**. *Byrne v. Trifillis*, 442 F.2d 1390, 170 USPQ 32, 34 (CCPA 1971). We believe that one following the Nelson disclosure would necessarily recognize that the compounds of the counts were disclosed as a combination that might be selected if desired, i.e., the message would be conveyed that Nelson invented the compounds of the counts.

Just as the Examiner is wrong as a matter of fact with his conclusory comments on the lack of interconnections and interrelations and combinations,[17] as with Byrne the Examiner is also wrong as a matter of law with his conclusory comments on the lack of interconnections and interrelations and combinations in view of the clear operability.

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16. Nelson v. Bowler, 1 USPQ2d 2076 at 2079 (Bd. Pat. App. & Int. 1986) (emphasis added).

17. The instant disclosure provides extensive relevant interconnections and interrelations and combinations including both hardware and software interconnections and interrelations and combinations.

1.5.4 The Disclosure Provides Actual Legal "Examples" Of The Interconnections

The disclosure is an integrated presentation of features that operate together and are interconnected together. For example: Fig. 1A is a top level block diagram with many of the components of the system disclosed and interconnected all-together; Figs. 1B, 1D-1G, 5A, 5D, and 6E are second level block diagrams detailing blocks in Fig. 1A; Figs. 1C, 1H-1J, 1L, 1P, 2M, 6A, 8, and 9 are simpler embodiment block diagrams illustrating subsets of and alternatives to Fig. 1A that can be used for different embodiments;[18] and Figs. 6B-6D and 6F-6AH are schematic diagrams still further detailing blocks in Fig. 1A. These figures present a significant amount of interconnections in between elements.

The computer listings (Spec. at 248-292, 544-574) are detailed source code Basic compiler listings. They are actually reduced-to-practice computer programs and they constitute "working examples". They are executed by the supervisory computer in the disclosed actually reduced-to-practice "Experimental System" and they operate with the other software (e.g., Basic compiler and C/PM operating system program) and hardware in the disclosed actually reduced-to-practice "Experimental System". Computer instructions in computer programs are expressly interconnected therebetween (Section 1.5.1 herein) and are expressly interconnected with the computer system on which they are being executed.

The "Overlays" section (Spec. at 386-406) further combines and interconnects claim limitations, the LD.ASC computer program still further combines and interconnects the image processing

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18. These include the block diagram (Fig. 1H) directed to the actually reduced-to-practice "Experimental System" ("Fig 1H is a block diagram of an alternate configuration of the system of the present invention as implemented in an experimental system" (Spec. at 5)).

operations, and the "image memory" are related operations yet further combine and interconnect the claim limitations.

If there is one thing that the instant disclosure has, it is interconnections and interrelations and combinations.

1.5.5 The Examiner Misrepresents The Interconnections And Interrelations Of Computer Programs

The Examiner disregards the interconnections and interrelations of computer programs. The computer programs have express interconnections and interrelations. See the discussions of the computer programs (Section 1.5.1 herein).

For example, the LD.ASC computer program, implements the actually reduced-to-practice features of generating graphics images and processed images and of overlaying, combining, and occulting of such features in image memory. The "Overlays" section is related to overlays of various types of image information (Spec. at 386-406). This section teaches overlaying of "combinations of processed images and graphic polygons" on a background (e.g.; Spec. at 386):

> Overlays
>
> Overlays can include combinations of processed images and graphic polygons. For example, in a map display; processed images can be used for background terrain and for certain objects overlayed thereon and graphic images can be used for symbols and polygon images overlayed thereon.

Then for twenty pages various combinations of overlays are discussed. The "Overlays" section expressly addresses overlaying of the following type images -- irregular cropped, perspective, warped, graphics, video, textured, and background images and expressly addresses rotation and translation for the overlay images.

The DIS.ASC computer program, implementing the actually reduced-to-practice features of the geometric processor, is disclosed as combining the features of: e.g.; geometric

processing (rotation, translation, expansion, and compression), wrapped-around image information, temporal interpolation, undersampling, display refreshing, and transforming. The DIS.ASC is disclosed as performing these operations on the image information stored in image memory; such as loaded with the image memory load computer program, overlaying with the LD.ASC program, and loading decompressed mosaics accessed from database memory. The geometric processor, is also disclosed as including 3D-perspective. Other disclosed features of the geometric processor include the following:

Table of Contents.

The FTR.ASC computer program is disclosed as combining the features of: e.g.; filtering, spatial interpolation, weighting and scaling, database memory, and mosaic processing. In a preprocessing embodiment, the FTR.ASC computer program is implemented as a preprocessor preprocessing image information for subsequent image processing (e.g., DIS.ASC image processing). Data compression and data decompression processing is also disclosed as being performed in the preprocessing embodiment.

The preprocessed image information can be loaded into image memory for overlaying with the LD.ASC computer program and for geometric processing and displaying with the DIS.ASC computer program.

The supervisory processor is disclosed as executing the DIS.ASC, FTR.ASC, LD.ASC, and GRAPH.ASC computer programs; interacting with system hardware and software (Fig. 1A); interconnected with system input and output devices, interconnected with geometric processors and spatial processors, have multiple interconnections with multiple channels, and interconnected with image memory (Figs. 1A and 1D). The supervisory processor is also disclosed as interacting with the disk database memory, operator controls, image memory, geometric processor, refresh memory, digital to analog converter, and display monitor (Fig. 1H); interacting with various additional system components (Figs. 1I and 1J); and interacting with the geometric processor registers (IC) which in turn interact with the image memory and the weight memory (Fig. 2I).

The image memory (disclosed in a 64-pixel block embodiment) is disclosed as storing image information involved in the execution of the DIS.ASC, LD.ASC, and GRAPH.ASC computer programs and from the preprocessor which includes data compressed, data decompressed, and image information filtered with the FTR.ASC computer program. The image memory is also disclosed as being interconnected with database memory and storing mosaics accessed from the database memory.

The discussion of the legal "examples" of computer programs further illustrate many of the interconnections. For example, the combination of rotating, translating, expanding, compressing, perspective, wrap-around, transform, temporal interpolation, and undersampling are all demonstrated with the geometric processor. Further, multiple channels, delta and difference image information, and feedback are all demonstrated with the geometric processor (e.g., Fig. 1A).

The "Overlays" section (Spec. at 386-406) discusses the combinations of hardware, software, image processing, and various types of image information.

The **original** Abstract, the **original** Summary Of The Invention, and the **original** claims provide significant combinations of features and interconnections therebetween. See the discussion of the original claims in Section 1.5.7 herein.

In addition to the extensive teaching of interconnections and interrelations of computer programs, the disclosure has extensive teachings of hardware and hardware/software interconnections and interrelations (briefly discussed below).

The disclosure includes tables of combinable features which are discussed in the disclosure in more detail. See the "MODULAR CONFIGURATION FEATURES TABLE" (Spec. at 24-30); the "EXPERIMENTAL CONFIGURATION FEATURES TABLE" (Spec. at 33); the "DIS.ASC TERMINOLOGY TABLE" (Spec. at 250-255); and the "IMAGE PROCESSING WORKSTATION TABLE" (Spec. at 485). The disclosure also includes the "COMPUTER PORT TABLE" (Spec. at 503) and the "PORT-C DESTINATION SELECT PORT" and "DESTINATION SELECT ASSIGNMENTS" (Spec. at 506-508).

The disclosure also includes the "CABLE CONNECTION TABLE" (Spec. at 510-521) showing system hardware interconnections. See the discussion of cable wire disclosure.

The disclosure is proliferated with teachings of the combinations and interconnections (e.g.; Spec. at 16 and 17-19; respectively):

> One configuration of the system of the present invention is an image processing system capable of geometrically manipulating a highly detailed image in true real time; such as for simultaneous rotation, translation, expansion, compression, 3D perspective, and warping at a 30-times per second update rate. Other capabilities include image enhancement, smoothing, and image filtering; all in real time. The image can be obtained from a wide variety of sources; such as from a video camera or from a database memory.
>
> The block diagram shown in Fig 1A illustrates the modular expandability of the system of the present invention, shown in greater detail in Figs 1B to 1G. A

plurality of geometric modules 110A to 110B can be configured in parallel channel form, such as for multiple overlays. The geometrically processed images can be combined with a geometric multiplexer/demultiplexer/combiner 110D. Multiplexing selects a particular geometric processed image channel for subsequent processing. Processing includes overlaying, adding, subtracting, and otherwise selecting and combining of images. For example, many channels of geometrically processed images 110C can be overlayed with occulting priorities. Also, a pair of images can be selected for arithmetic processing, such as for adding together.

The processed and combined images can be demultiplexed with element 110D to route the appropriate images to the appropriate spatial modules 110E to 110F and for feedback to the geometric modules along path 110H. The spatial modules 110G can be implemented in parallel form for processing the images routed thereto. A spatial multiplexer and demultiplexer 110I can be used to multiplex and demultiplex the spatially processed images from spatial modules 110G for outputting.

A plurality of input sources of images 110J and a plurality of output devices for images 110K can be accommodated. The input images from input sources 110L can be processed with the input interfaces 110M and processed with a multiplexer/demultiplexer 110N for routing to geometric modules 110C. Output devices 110K can be excited with images that are processed with the output image interfaces 110P and output multiplexer/demultiplexer 110Q.

Multiplexer/demultiplexer modules 110D, 110N, and 110Q can be implemented to multiplex a plurality of channels into one channel and then to demultiplex that one channel into a plurality of channels. Each multiplexer associated with a channel can be replicated a plurality of times to multiplex a plurality of channels into each single channel. The multiplex signals associated with the plurality of multiplexed channels can then be demultiplexed, permitting routing of any one of a plurality of multiplexer input channels to any one of a plurality of multiplexer output channels. Tri-state multiplexers can be used to multiplex a plurality of channels into a single channel, such as using 74LS365 multiplexer circuits. Parallel fanout and gating networks can be used for demultiplexing. Other types of multiplexers and demultiplexers are well-known and can be used for the multiplexer/demultiplexer modules.

A supervisory processor 110R provides supervisory operations; such as receiving external commands 110S for configuring the system. For example, geometric modules 110C can be controlled for different types of geometric processing with different geometric parameters; spatial modules 110G can be controlled for different types of weights loaded into weight RAMs; and the

multiplexer/demultiplexer modules and combiner module 110I, 110N, and 110Q can be selected for multiplexing and demultiplexing of images.

1.5.6 The Disclosure Provides Such Extensive Interconnection And Interrelation Details That It Even Includes Details Of Cable Wires

The instant disclosure is so detailed that it includes significant details for the actually reduced-to-practice "Experimental System" -- e.g.; detailed schematic diagrams (Figs. 6B-6AH), integrated circuit component placement on the circuit boards (Spec. at 522-543), actual wiring between the integrated circuit components (Figs. 6B-6AH), details of cable wires between system components (Spec. at 510-521), and the detailed computer program source code listings (Spec. at 544-574):

Table of Contents.

Cable List

A cable list is provided in the CABLE CONNECTION TABLE included herewith. This cable list identifies the cables between the various Vector boards and between the Vector boards and the supervisory processor. Each cable between display processor boards is implemented with a 50-pin ribbon cable having odd pins connected to ground for signal isolation. Each cable between the Vector boards and the supervisory processor is implemented with an RS-232 type 25-pin ribbon cable, consistent with the signal representations for the Compupro Interfacer-II board. The cable list identifies the pin associated with a signal, a symbol associated with the signal, a description of the signal, a representative source of the signal and a representative destination of the signal.

Spec. at 295.

Despite the significant efforts that the Appellant went through to develop and test the actually reduced-to-practice "Experimental System" and then to disclose it in significant detail in the instant application, the Examiner has failed to properly consider this very relevant and detailed disclosure.

1.5.7 The Image Memory Provides Extensive Interconnections And Interrelations

The image memory is a prominent part of the actually reduced-to-practice "Experimental System", as discussed below. The image memory provides "working examples" of overlaying, image processing, and displaying of image information. Hence, the image memory by itself provides "working examples" and express teachings for the interconnections and interrelations between the claim limitations.

The term "image memory" occurs more than 300 times in the disclosure.

The image memory is discussed with many of the disclosed features. For example, the "Overlay" section expressly teaches the image memory for overlaying many different types of image information. A single one of the various image memory related

excerpts from this single "Overlays" section, together with various different types of image information overlaid therewith, is set forth below (e.g.; Spec. at 390-391 (emphasis added)):

> Graphic overlays that are independent of textured images and that are processed independently of other images will now be discussed. Graphic overlays can be written into a separate graphic **image memory**. This graphic image can be geometrically processed, as discussed for processing of textured images in **image memory**. The geometrically processed image can be output for display, can be overlayed on other graphic images and processed images in other image memories, and can be otherwise processed as discussed for processing of textured images herein.
>
> Graphic overlays that are fixed in the viewport will now be discussed. Graphic overlays can be written into a separate graphic **image memory**. These graphic overlays can be referenced to the viewport and can be fixed to the viewport; such as with a viewport frame, alphanumeric characters, and other features that are to remain stationary in the viewport. This fixed graphic image can be scanned-out of the related **image memory** in raster scan form without rotation, translation, expansion, compression, or other geometric processing.

As another example, the "Overlays" section teaches use of "image memory" for overlaying (and combining, occulting, compositing, and multiplexing) of images and for the processing of these images. The "Image Loading" section (Spec. at 246) provides "working examples" of the loading of picture images into "image memory", the LD.ASC computer program (Spec. at 547-60) provides "working examples" of the loading of graphic images and processed images into "image memory" and provides "working examples" of the overlaying of the images stored in "image memory" therewith, the DIS.ASC computer program (Spec. at 248-292, 567-574) provides "working examples" of the rotation, translation, expansion, and compression of images stored in "image memory". The "Database Data Compression" section (Spec. at 435-438) provides "examples" of data compression and data decompression of images stored in "image memory". Some of the excerpts from the disclosure regarding these features are discussed below. Various other "examples" of the use of "image

memory" are provided in the disclosure -- "image memory" terminology occurs verbatim more than 300 times in the disclosure.

As another example, image memory is expressly addressed in the "Overlays" section. There are 16 occurrences of the term "image memory" in the "Overlays" section. This is included in the more than 300 occurrences of the term "image memory" in the disclosure. An example of occurrences in the "Overlays" section is excerpted below (e.g.; Spec. at 389 (emphasis added)):

> Graphic overlays that are associated with images and geometrically processed with such associated images will now be discussed. Graphic overlays can be written over an image in **image memory** to provide a permanent overlay. Such permanent overlays have been demonstrated with the BASIC PROGRAM LISTING LD.ASC Basic provided herein by loading graphic vectors, rectangles, and test patterns and by loading textured image test patterns over an image in **image memory**.

In view of the above, the "Overlays" section provides clear "working examples" of the overlaying over the images that have been loaded into "image memory" and the processing of images that have been loaded into "image memory". Further, the "Overlays" section provides clear "working examples" of the overlaying over the images into a memory having the features of "image memory"; e.g., the 64-pixel blocks of this "image memory" embodiment.

The "Image Loading" section (Spec. at 246) provides "working examples" of the loading of picture images into "image memory" (e.g.; Spec. at 246 (first emphasis in original, all other emphasis added)):

> Image Loading
>
> Loading of an image into memory is performed by loading the XP and YP-address registers with the address of each pixel to be loaded, then outputting the pixel information to be loaded with Port-B, and then strobing the pixel information into **image memory** with the DOA7 signal. A sequential load feature is provided under control of the DOA5 signal. When the DOA5 signal is high, a vector can be loaded; where the previously loaded pixel address is incremented with the related delta parameter to obtain the next pixel address to reduce software overhead and thereby speedup loading of **image memory**.

Loading of **image memory** with the supervisory processor is performed with a 3-port output arrangement having 8-bits per port. The first port, Port-A, communicates control signals between the supervisory processor and the display processor. The second port, Port-B, communicates address and data information to be loaded into the display processor between the supervisory processor and the display processor. The third port, Port-C, selects the register or memory in the display processor for loading. The protocol involves outputting of the destination address on Port-C, outputting of information to be loaded into the display processor on Port-B, and then outputting of a data strobe on Port-A. The data strobe loads the output information into the selected destination.

A program to load vectors into memory is provided herein as the BASIC PROGRAM LISTING LD.ASC and is briefly discussed in the section entitled Software herein.

The LD.ASC computer program (Spec. at 547-560) provides "working examples" of the loading of graphic images and processed images into "image memory" and provides "working examples" of the overlaying of the images stored in "image memory" therewith (e.g.; Spec. at 155-158, and 389 (first emphasis in original, all other emphasis added)):

GRAPHICS PROCESSOR

A graphics processor architecture can be implemented with a address generator and control logic generating graphics vectors for storing into **image memory**. **Image memory** can then be scanned out, such as in a raster scan form to refresh a display. In one configuration, graphics vectors can be written into **image memory** on an offline basis and can be used to refresh the display on an online basis. Alternately, graphics vectors can be written into **image memory** on an online basis time shared with refreshing of the display on an online basis.

One arrangement of the graphics system of the present invention is shown in Fig 1. Supervisory processor 115A loads graphics commands into address generators 115B. Address generators 115B generate addresses of graphics vectors for loading into **image memory** 115C and for raster scanning **image memory** 115C. The raster scan addresses scan-out the image in **image memory** 115C through the CRT interface 115D to refresh CRT 115E.

An experimental system has been constructed to demonstrate operation of the graphics display capability. The arrangement shown in Fig 1 has been implemented in hardware for refreshing the display in real time. A program, such as the BASIC PROGRAM LISTING GRAPH.ASC, can be used to control that experimental hardware for

refreshing the display. In this experimental system, the graphics vectors are loaded in an offline manner with the **LD.ASC Basic program** set forth in the **BASIC PROGRAM LISTING LD.ASC** herein; emulating hardware loading of graphics vectors in an online manner. In this experimental system, graphics operation is initiated each frame with supervisory processor 115A and hardware refresh is performed with address generators 115B and **image memory** 115C....

The address generators can be used to generate graphic vectors and windows. For example, the **LD.ASC program** set forth in the **BASIC PROGRAM LISTING LD.ASC** herein has been used to load graphic vectors into **image memory**. This is achieved by using the address generators to generate the addresses of a vector and by strobing the color intensity of the vector into **image memory**.

Graphic overlays can be written over an image in **image memory** to provide a permanent overlay. Such permanent overlays have been demonstrated with the **BASIC PROGRAM LISTING LD.ASC** Basic provided herein by loading graphic vectors, rectangles, and test patterns and by loading textured image test patterns over an image in **image memory**.

Loading and overlaying into image memory is also taught in the LD.ASC computer program (e.g.; Spec. at 548 (emphasis added)):

```
120   PRINT "SELECT OVERLAY FOR LOADING INTO IMAGE MEMORY ... 1"
122   PRINT "SELECT IMAGE TO BE LOADED INTO IMAGE MEMORY"
124   PRINT "       CONCENTRIC SQUARE FRAMES ..... 2"
126   PRINT "       RECTANGLES AND LINES ..... 3"
128   PRINT "       SPIRALS ..... 4"
130   PRINT "       VIEWPORT COORDINATE SYMBOLS ..... 5"
132   PRINT "       PATTERN #6 ..... 6"
134   PRINT "       PATTERN #7 ..... 7"
136   PRINT "       SQUARE PATTERN  ..... 8"
138   PRINT "       SQUARE FRAMES ..... 9"
140   PRINT "       PERIPHERAL SQUARES ..... 10"
141   PRINT "       PERIPHERAL TRIANGLES ..... 11"
142   PRINT "       HOUSE ..... 12"
151   INPUT "              SELECT OPERATION NUMBER";A20%
152   IF A20%<13 THEN 155
153   PRINT "****************": PRINT "IMPROPER SELECTION":
          PRINT "***************"
154   GOTO 112
155   IF A20%>0 THEN 158
156         SYSTEM
158   ON A20% GOSUB 170, 4400, 4530, 5500, 4500, 7500, 8500, 9000, 9040,
        9180, 9280, 11070
159   GOTO 112
```

```
170   PRINT: PRINT "***************************************************"
171   PRINT "   SELECT OVERLAY FOR LOADING INTO IMAGE MEMORY"
172   PRINT "***************************************************": PRINT
173   PRINT "  RETURN TO MAIN MENU ..................... 0"
174   PRINT "  SELECT RECTANGULAR IMAGE MEMORY PATTERN"
180   PRINT "      HORIZONTAL BARS"
200   PRINT "         3-2-2 WIDTH BARS, INTENSITY VARATIONS . 1"
220   PRINT "         1-1-1 WIDTH BARS, MAXIMUM INTENSITY ... 2"
240   PRINT "         LINEAR COUNT, ALL COLOR COMBINATIONS .. 8"
260   PRINT "      SOLID SINGLE COLORED IMAGES"
265   PRINT "         RECTANGLE ............................ 3"
270   PRINT "         BACKGROUND ........................... 4"
400   PRINT "      CHECKERBOARD"
420   PRINT "         4-COLORS ............................. 6"
440   PRINT "         2-COLORS ............................. 7"
442   PRINT "      VARIABLE SINGLE COLORS"
443   PRINT "         GREEN SAWTOOTH ....................... 10"
460   PRINT "      CENTER ELEMENT"
480   PRINT "         9-PIXEL SQUARE ....................... 11"
482   PRINT "  SELECT SLOPING LINE ......................... 12"
484   INPUT "                                  SELECT PATTERN NUMBER";A5%
486   IF A5%>0 THEN 502
```

The DIS.ASC computer program (Spec. at 248-292, 567-574) provides "working examples" of the rotation, translation, expansion, and compression of images stored in "image memory" (e.g.; Spec. at 262-263, 278-279, and 375 (emphasis added)):

> The following code defines the **image memory** dimensions; which are 512-pixels per line (X5I) and 512-lines per image (Y5I) for this implementation.
>
> ```
> 1080   X5I=512: Y5I=512  'IMAGE MEMORY DIMENSIONS IN PIXELS
> ```
>
> The following code represents calculations for geometric window relationships. These relationships pertain to prior window configurations, which are discussed with reference to Figs 2C, 2D, and 2G. Because these relationships represent prior relationships, they are deleted with apostrophes and maintained as annotations.
>
> ```
> 1100  'A       R1=SQR(X5V^2+Y5V^2)      'UNITS OF PIXELS
> 1120  'A       AP1=ATN(Y5V/X5V)
> 1140  'A       A6=ATN(X5V/Y5V): AP1=90*DR-A6
> ```
>
> The following code defines the **image memory** dimensions in eighth pixel units by multiplying the **image memory** dimensions X5I and Y5I by 8-eighth pixel units.
>
> ```
> 1160   KS1%=X5I*8: KS2%=Y5I*8  'IMAGE MEMORY DIMENSIONS
>     IN EIGHTH PIXELS
> ```
>
> The following code defines parameters Q2 and Q3 in terms of the viewport dimensions and in terms of the offset of the center of rotation.

```
1180   Q2=(Y5V/2)-TY: Q3=(X5V/2)+TX
```

The following code calculates the window parameters for the selected window geometry.

```
1200   IF PR32$="Y" GOTO 1260
1220   AP1=ATN(Q2/Q3): R1=2*SQR(Q2^2+Q3^2)
1240    KB1=R1*8*SIN(AP1)/2: KB2=R1*8*COS(AP1)/2: GOTO 1280
1260   KB1=Q2*8: KB2=Q3*8
```

The following code defines initial conditions for scaling prior to receipt of joystick commands.

```
1280   DS11=1: JSS%=128
```

The following code calculates the initial conditions for the center of the **image memory**, XC1 and YC1, relative to the center of the viewport and rescales the center coordinates, XC1 and YC1, and offset parameters, TX and TY, to subpixel units with the multiplication by eight.

```
1300   XC1=(X5I/2+X1)*8: YC1=(Y5I/2+Y1)*8: TX=TX*8:
TY=TY*8
```

The following code calculates the resolved joystick translation commands. The joystick commands are implemented to be in viewport coordinates. Consequently, rotation of the image rotates the image in the **image memory** relative to the viewport, where the joystick translation axis, which are **image memory** coordinate related, also rotate. In order to reference the translation axes to the viewport coordinates, the joystick translation commands are be resolved from **image memory** coordinates into viewport coordinates by summing the resolved components from the **image memory** coordinates to obtain the translation commands in viewport coordinates.

```
3600   JSYK%=JSYB%*KSAR: JSXK%=JSXB%*KSAR
3620   JSXB%=JSXB%*KCAR+JSYK%: JSYB%=JSYB%*KCAR-JSXK%
```

The image received from the source of the image can be buffered in a buffer memory for preprocessing. The buffered image can be loaded into **image memory** for geometric processing when the geometric processing goes beyond the limits of the image stored in **image memory**. For example, when the image in **image memory** is to be translated past a boundary of **image memory**, or is to be compressed below a compression threshold, or otherwise processed beyond the limits of the image; the buffered image can be loaded into **image memory** to continue geometric processing.

The "Database Data Compression" section (Spec. at 435-438) provides "examples" of data compression and data decompression of images stored in "image memory" (e.g.; Spec. at 437 (emphasis added)):

Compressed information can be **decompressed** prior to loading into **image memory** so that images in **image memory**

are in **decompressed** form. Alternately, **compressed** information can be stored in **image memory** and can be **decompressed** when processed as an output of **image memory**. **Geometric processing can be performed on decompressed information stored in image memory**; where **decompression** can be performed prior to geometric processing, such as before loading into image memory or after accessing from image memory. Geometric processing can be performed on **compressed** information in **image memory**; where **decompression** can be performed subsequent to geometric processing, such as before spatial processing or after spatial processing.

The **original** claims address image memory for machine vision, for storing a reference image, for storing a part of a database image, for processing the image stored in the image memory, for geometrically processing -- compressed, expanded, rotated, translated, warped, and perspective -- the image stored in image memory (emphasis added):

> 3. A machine vision system comprising:
> means for acquiring an input image;
> means for storing a reference image;
> means for registering the input image and the reference image;
> means for comparing the registered input image and reference image; and
> means for generating an output signal in response to the comparing with said comparing means.
>
> 4. The system as set forth in claim 3 above, wherein said acquiring means is a video camera for acquiring the input image, wherein said storing means is an **image memory** for storing the reference image, wherein said registering means is a geometric processor for rotating, translating, and scaling the input image to cause the input image to register with the reference image, and wherein said comparing means is a spatial filter for comparing the registered input image and reference image; said system further comprising artificial intelligence means for processing the output signal.
>
> 5. A system for processing an image comprising:
> a database for storing a database image;
> an **image memory** for storing a portion of the database image;
> memory loading means for loading a portion of the database image into said **image memory** including means for scrolling the database image into said **image memory** to provide image motion; and

a processor for processing the image stored in said **image memory** to provide a processed image.

6. The system as set forth in claim 5 above, wherein said database includes a digital memory for storing a database image having more than 10-million pixels, wherein said **image memory** includes means for storing a portion of the database image having less than 2-million pixels, wherein said memory loading means includes means includes a processor operating under control of a memory management program for loading a portion of the database image into said **image memory**, and wherein said processor includes means for geometrically processing the image stored in said **image memory** to provide a geometrically processed image, means for spatially processing the geometrically processed image from said image processor to provide a geometrically and spatially processed image, and display means for displaying the geometrically and spacially processed image.

7. A geometric processor comprising:
means for storing an image;
means for scanning out the image stored in said storing means;
means for displaying the image scanned out with said scanning out means.

8. The processor as set forth in claim 7 above, wherein said storing means includes an **image memory** for storing the image in memory map form, wherein said scanning out means includes means for scanning out the image stored in said **image memory** at an angle to provide a rotated scanned out image, and wherein said displaying means includes means for displaying the image scanned out with said scanning out means as a rotated image.

9. The processor as set forth in claim 7 above, wherein said storing means includes an **image memory** for storing the image in memory map form, wherein said scanning out means includes means for scanning out the image stored in said **image memory** at greater than pixel sampling steps to provide a compressed scanned out image, and wherein said displaying means includes means for displaying the image scanned out with said scanning out means as a compressed image.

11. The processor as set forth in claim 7 above, wherein said storing means includes an **image memory** for storing the image in memory map form, wherein said scanning out means includes means for scanning out the image stored in said **image memory** at less than pixel sampling steps to provide an expanded scanned out image, and wherein said displaying means includes means for

displaying the image scanned out with said scanning out means as an expanded image.

12. The processor as set forth in claim 7 above, wherein said storing means includes an **image memory** for storing the image in memory map form, wherein said scanning out means includes means for scanning out the image stored in said **image memory** at varying pixel sampling steps to provide a warped scanned out image, and wherein said displaying means includes means for displaying the image scanned out with said scanning out means as a warped image.

13. The processor as set forth in claim 7 above, wherein said storing means includes an **image memory** for storing the image in memory map form, wherein said scanning out means includes means for scanning out the image stored in said **image memory** at range variable pixel sampling steps to provide a 3D perspective scanned out image, and wherein said displaying means includes means for displaying the image scanned out with said scanning out means as a 3D perspective image.

14. The processor as set forth in claim 7 above, wherein said storing means includes an **image memory** for storing the image in memory map form, wherein said scanning out means includes means for scanning out the image stored in said **image memory** at a range variable angle to provide a 3D perspective scanned out image, and wherein said displaying means includes means for displaying the image scanned out with said scanning out means as a 3D perspective image.

The image memory is significantly related to the database memory and mosaics in the disclosed actually reduced-to-practice "Experimental System".

The image memory has significant relevant disclosure, as discussed above. It is disclosed as part of the actually reduced-to-practice "Experimental System" which includes "working examples" of hardware embodiments and which includes computer source code for various claim limitations. It provides important intraconnections and intrarelations between computer programs, between hardware, and between image information and it provides important interconnections and interrelations between computer programs, hardware, and image information.

1.6 The Examiner's Enablement References Contradict The Enablement Rejection

The Examiner's enablement references contradict the enablement rejection. The Examiner cites to Sullivan, Rogoff, Hudson, and Egeli to attempt to create a low skill in the art and lack of enablement issue, but this position is erroneous. These references contradict the enablement rejection.

First, drawing self-serving conclusions from Sullivan, Rogoff, Hudson, and Egeli does not establish the skill in the art nor lack of enablement in the instant application. These references provide discretionary disclosures, they are not authorities regarding the "requirements" for enablement. To the contrary, the law on enablement provides the requirements and authorities for enablement.

Second, Hudson and Egeli are articles that bear no presumption of enablement or other credible basis for the Examiner's conclusions.

Third, as an example, these references lack the detailed schematic diagrams provided in the instant disclosure. The general block diagrams in Sullivan, Rogoff, and Egeli and the absence of even a block diagram in Hudson contradict the Examiner's position. In contrast, the instant application discloses not only detailed block diagrams in a top-down end-to-end format but provides detailed schematic diagrams.

Fourth, as another example, these references lack the detailed theoretical background provided in the instant disclosure. The sparse equations, cartoons, and discussions in these references hardly match the derivation of the window geometries (e.g., Figs 2A-2G, Spec. at 75-93) and the other disclosures of the theoretical background provided in the instant disclosure. For example, see Sullivan's terse cartoon (Fig. 2A) and Rogoff's terse cartoons (Figs. 1 and 2). In contrast, the instant disclosure provides extensive theoretical background for the software and hardware implementations.

Fifth, as still another example, Rogoff, clearly uses a computer 20 (Fig. 3) but lacks disclosure of a computer flow diagram as provided in the instant disclosure. In contrast, the instant disclosure provides extensive discussions of a computer flow diagram and a state diagram.

Sixth, as yet another example, these references use what appear to be blocks designed specifically for the systems, yet the instant disclosure incorporates many commercially available products (in addition to specifically designed software and hardware) ranging from commercially available integrated circuits to a commercially available computer and computer operating system software.

Seventh, as yet another example, detailed input and output software (e.g.; in source code and with a commercially available operating system program) and input output hardware (e.g.; with detailed schematic diagrams and with commercially available computer input/output circuit cards).

Eighth, the skill in the art was sufficient to enable an artisan to practice the invention by merely disclosing "the functions of the software" (Section 1.7 herein).

In view of the above, these references contradict the enablement rejection. Hence, the enablement rejection should be withdrawn.

1.7 The Examiner Misrepresents The Skill In The Relevant Arts

It is well established by the courts and by a recent decision of the Board in a related application that the skill in the arts relevant to the instant disclosure is high. See, e.g.; below and at Sections 1.14.3 - 1.14.5 herein. Thus, for this reason alone, the Examiner's position -- that the skill in the art was low -- confirms that the enablement rejection fails to establish a prima facie case.

Even though not necessary, the Applicant has disclosed in great detail a reduced-to-practice "Experimental System" that

provides significant guidance to an artisan. Applicant has also disclosed video tapes in Disclosure Documents filed in the PTO showing operation of the reduced-to-practice system.

The Board in a copending application reversed an enablement rejection stating:[19]

> ... the fact that limitations are not described does not establish that it would take undue experimentation for one of ordinary skill in the art to make what is claimed. **The level of skill in the pertinent arts of computers, memory architecture, and computer programs was high**. Although the Wands factors are only for guidance, the examiner has not provided any explanation of why one of ordinary skill could not make the broadly claimed subject matter without undue experimentation. We conclude that the examiner has failed to make out a prima facie case of lack of enablement, not that the claimed subject matter is enabled.

The courts have established the high skill in the relevant arts at an early time in the evolution in the relevant arts. For example, the court in Scarbrough, stated:[20]

> We have previously held in Hayes and in Fonar (after the district court decided this case) that when disclosure of software is required, **it is generally sufficient if the functions of the software are disclosed**, it usually being the case that creation of the specific source code is within the skill of the art ....

The filing date of the application involved in Scarbrough was October 18, 1968, long before the instant effective filing date.

Further, the court in Hayes stated:[21]

> One skilled in the art would know how to program a microprocessor to perform the necessary steps described in the specification. Thus, an inventor is not required to describe every detail of his invention. An applicant's disclosure obligation varies according to the art to which the invention pertains. Disclosing a microprocessor

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19. Appeal No. 2002-0652, Decision at 32-33 (emphasis added).

20. In re Scarbrough, 500 F.2d 560, 182 USPQ 298 (CCPA 1974) (emphasis added).

21. In re Hayes, 982 F.2d 1527, 25 USPQ2d 1241 (Fed. Cir. 1992).

capable of performing certain functions is sufficient to satisfy the requirement of section 112, first paragraph, when one skilled in the relevant art would understand what is intended and know how to carry it out.

The filing date of the application involved in Hayes was June 19, 1981.

Still further, the court in Fonar stated:[22]

> As a general rule, where software constitutes part of a best mode of carrying out an invention, **description of such a best mode is satisfied by a disclosure of the functions of the software**. This is because, normally, writing code for such software is within the skill of the art, not requiring undue experimentation, once its functions have been disclosed. It is well established that what is within the skill of the art need not be disclosed to satisfy the best mode requirement as long as that mode is described. Stating the functions of the best mode software satisfies that description test. We have so held previously and we so hold today .... Thus, flow charts or source code listings are not a requirement for adequately disclosing the functions of software.

The filing date of the application involved in Fonar was March 17, 1972.

As recently as 2004, the Federal Circuit in Chiron stated:[23]

> Moreover, the prior application must enable one of ordinary skill in the art to practice `the full scope of the claimed invention.' In re Wright .... Clarifying this principle, this court has explained: `That is not to say that the specification itself must necessarily describe how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can often fill gaps, interpolate between embodiments, and perhaps even extrapolate beyond the disclosed embodiments, depending upon the predictability of the art.'

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22. Fonar v. General Electric, 107 F.3d 1543, 41 USPQ2d 1801 (Fed. Cir. 1997) (emphasis added).

23. Chiron v. Genentech, 70 USPQ2d 1321 at 1325 (Fed. Cir. 2004).

Still further, the CCPA in Bowen stated:[24]

> As we explained in In re Fisher, 57 CCPA at 1108, 427 F.2d at 839, 166 USPQ at 24:
> **In cases involving predictable factors, such as** mechanical or **electrical elements**, a single embodiment provides broad enablement in the sense that, once imagined, other embodiments can be made without difficulty and their performance characteristics predicted by resort to known scientific laws. In cases involving unpredictable factors, such as most chemical reactions and physiological activity, the scope of enablement obviously varies inversely with the degree of unpredictability of the factors involved.

Of course, this discussion would not be complete without addressing Sherwood. The filing date of the application involved in Sherwood was April 14, 1975.

The CCPA in Sherwood established that "the touchstone [for § 112-1] is the content, not the form", and that § 112-1 can even be satisfied with a "verbal flow chart":[25]

> Taking into account the expert opinions found in the two affidavits, it would appear that the detailed disclosure of the analog method in combination with the suggestion that a digital method should be used might be more enlightening to one having ordinary skill in the art than the computer listing or flow chart required by the PTO. We view the PTO's requirement as quite formalistic in view of the **verbal flow chart** provided by appellant in the specification. In any event, **the touchstone is the content, not its form**.

The CCPA in Sherwood then applied this century-old Supreme Court wisdom to computer programming:

> In general, writing a computer program may be a task requiring the most sublime of the inventive faculty or it may require only the droning use of a clerical skill. The difference between the two extremes lies in the creation of mathematical methodology to bridge the gap between the information one starts with (the "input") and the

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24. In re Bowen, 492 F.2d 859, 181 USPQ 48 at 50 (CCPA 1974).

25. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544-545 n.8 (CCPA 1980) (emphasis added).

information that is desired (the "output"). If these bridge-gapping tools are disclosed, there would seem to be no cogent reason to require disclosure of the menial tools known to all who practice this art.

Sherwood.[26]

In assessing any computer-related invention, it must be remembered that the programming is done in a computer language. The computer language is not a conjuration of some black art, it is simply a highly structured language. Analogously, if a person were to express a complete thought in German, it would be no trick for a translator to convert that thought into a palpable English form. The thought, thus expressed, might not be worthy of Shakespeare, but it would be understandable to one who uses the English language. Similarly, the conversion of a complete thought (as expressed in English and mathematics, i.e., the known input, the desired output, the mathematical expressions needed and the methods of using those expressions) into the language a machine understands is necessarily a mere clerical function to a skilled programmer.

Sherwood.[27]

Taking into account the expert opinions found in the two affidavits, it would appear that the detailed disclosure of the analog method in combination with the suggestion that a digital method should be used might be more enlightening to one having ordinary skill in the art than the computer listing or flow chart required by the PTO. We view the PTO's requirement as quite formalistic in view of the verbal flow chart provided by appellant in the specification. In any event, the touchstone is the content, not its form.

Sherwood.[28]

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26. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544 (CCPA 1980).

27. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544 n.6 (CCPA 1980).

28. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544-545 n.8 (CCPA 1980).

In view of the above -- the skill in the relevant art was high and the disclosure has far more than is necessary with an actually-reduced-to-practice embodiment -- the enablement rejection should be withdrawn.

1.8 The So-Called "Example" Claim Selected By The Examiner

The Examiner selects a so-called "example" claim (claim 554) regarding the '112-1 rejections. However, this claim is not representative of many of the other claims. Further, this claim clearly has adequate written description and is clearly enabled. See, e.g.; the following reading on Fig. 1A.

> 554. A process comprising the acts of:
>
> storing computer instructions (e.g.: Fig. 1A, 110R; Spec. 24, 243-292, 544-574);
>
> generating GPS navigation information in response to the computer instructions (e.g.: Fig. 1A, 110A-110C, 110R; Fig. 1D, 111C; Spec. 24, 27, 387-389, 547-560);
>
> generating radar information (e.g.: Fig. 1A, 110L, 110M; Spec. 25, 49-50, 70);
>
> generating feedback information in response to the computer instructions and in response to the radar information (e.g.: Fig. 1A, 110H; Spec. at 24-27);
>
> generating data compressed image information in response to the computer instructions and in response to the radar information (e.g.: Fig 1A, 110K; Fig. 1G, 113K, 113L; Spec. 16, 22, 31-32, 407-438); and
>
> writing database information into a database memory in response to the computer instructions and in response to the radar information (e.g.: Fig. 1A, 1G; Spec. 16, 22, 31-32, 407-438).

1.9 The Examiner Did Not Even Get Started On His § 112-1 Examination According To The Courts And The PTO

The Examiner did not even get started on his § 112-1 examination according to the courts and the PTO.

According to the PTO, the starting point must be the working example and the Examiner "**must**" then "extrapolate" from the working example "across the entire scope of the claims" (see below). However, the Examiner did not even consider the Applicant's working examples (discussed herein). Hence, the Examiner could not possibly have started with the working examples as required and he certainly could not have extrapolated from the working example "across the entire scope of the claims" as further required. See MPEP 2164.02:

> To make a valid rejection, one must evaluate all the facts and evidence and state why one would not expect to be able to extrapolate that one example across the entire scope of the claims.

The PTO position is supported by the courts.[29] The starting point (the "outset") in this case is the instant disclosure, including the disclosed actually reduced-to-practice "Experimental System". From this starting point, the Examiner "**must**" establish "some technical uncertainty". However, as discussed above, the Examiner never got to the starting point, never properly evaluated the disclosed actually reduced-to-practice "Experimental System", and never established any "technical uncertainty" starting with the disclosed actually reduced-to-practice "Experimental System".

The court in United Stationers stated:

> H.R. Conf. Rep. No. 99-841, at II-72 (1986).... The Report suggests that qualifying research **must from its outset**

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29. Norwest Corporation and Subsidiaries v. Commissioner of Internal Revenue, 110 TC 454, 507-508 (1998); WICOR, Inc., and Subsidiaries v. United States, 116 F. Supp. 2d 1028, 1035-36 (E.D. Wis. 2000); United Stationers, Inc. v. United States, 163 F.3d 440, 445-46 (7th Cir. 1998).

> **involve some technical uncertainty** about the possibility of developing the product. See *Norwest, 1998 U.S. Tax Ct. LEXIS 32, P 52,758, at 4655* (discussing the "required uncertainty"); cf. *TSR, 96 T.C. at 920-21.*

163 F.3d at 446 (emphasis added). However, the Examiner has not established "some technical uncertainty about the possibility of developing the product" -- which is the making or using of the invention. This is not surprising -- what could the Examiner say about a technical uncertainty of making or using software, or making and using a memory, or purchasing a display monitor particularly when the disclosed actually reduced-to-practice "Experimental System" had already been developed and was the starting point -- the "outset".

According to the Federal Circuit, the starting point must also include construing the claims, but the Examiner has not construed the claims. For example, in Gechter, Judge Michel clarified claim construction:

> Implicit in our review of the Board's anticipation analysis [and any other patentability analysis] is that the claim **must first have been correctly construed** to define the scope and meaning of each contested limitation.

Gechter at 1032.

In view of the above, the Examiner did not even get started on his § 112-1 examination.

1.10 The Description More Than Satisfies The Law On Written Description

Written description involves whether each contested claim **limitation** can be found in the disclosure:[30]

> In order to satisfy the written description requirement ... one skilled in the art, reading the original disclosure, must "immediately discern **the limitation at issue**" in the claims.

Purdue Pharma.[31]

> Any time an examiner bases a rejection ... on the lack of a written description, the examiner should: (A) identify **the claim limitation** not described; and (B) provide reasons why persons skilled in the art at the time the application was filed would not have recognized the description of **this limitation** in the disclosure of the application as filed.

MPEP 2163.04 (emphasis added).

> To comply with the written description requirement of 35 U.S.C. 112, ¶ 1 ... **each claim limitation** must be expressly, implicitly, or inherently supported in the originally filed disclosure.

PTO Guidelines at Section II.A.3.a,(2)b.[32]

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30. The rule for the written description requirement is that it should be **reasonably** applied and that the disclosure of the claim limitations need not be verbatim, but can be implicit or inherent.

31. Purdue Pharma v. Faulding, 230 F.3d 1320, 56 USPQ2d 1481, 1483 (Fed. Cir. 2000) (emphasis added); see also Waldemar Link GmbH & Co. v. Osteonics Corp., 32 F.3d 556, 558, 31 USPQ2d 1855, 1857 (Fed. Cir. 1994).

32. Guidelines for the Examination of Patent Applications Under the 35 U.S.C. 112, ¶ 1, "Written Description" Requirement; Official Gazette 1242 O.G. 168 (January 30, 2001) (emphasis added).

The CCPA in both Angstadt and Moore held that the written description requirement is relatively simple to comply with:[33]

> Two of the first paragraph requirements indicated above, i.e., **the "description of the invention"** and the "best mode" requirements, **are relatively simple to comply with and thus will ordinarily demand minimal concern on the part of the Patent Office** * * * What is of maximum concern in any analysis of whether a particular claim is supported by the disclosure in an application is whether that disclosure contains sufficient teaching regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and to use the claimed invention.

However, the Examiner disregarded the CCPA's directive -- that the written description requirement is "relatively simple to comply with and thus will ordinarily demand minimal concern on the part of the Patent Office".

The Federal Circuit confirmed that the **only** disclosure needed for a firmware embodiment is the "general function of the firmware":

> While we agree that the '302 patent **only** discloses the **general function** of the firmware without teaching mathematical formulas, flow charts, or a firmware program listing, **no more was needed here**.

Hayes.[34]

> The solicitor's reliance on what this court has referred to as the "description requirement" of the first paragraph of § 112 is misplaced. The so-called "description requirement," which exists in the first paragraph independent of the enablement (how to make and how to use) portions, serves essentially two functions.... Both are fully defeated by a specification, which **describes the invention in the same terms as the claims**. Here there has been no assertion by the board or the examiner that there is any lack of **correspondence between the appealed claims**

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33. In re Angstadt and Griffin, 537 F.2d 498, 190 USPQ 214, 217 (CCPA 1976). In re Moore, 439 F.2d 1232, 169 USPQ 136, 239 (CCPA 1971).

34. In re Hayes Microcomputer Products Inc., 982 F.2d 1527, 25 USPQ2d 1241, 1248 (Fed. Cir. 1992) (emphasis added).

> **and the specification** (including the original claims) as filed. Indeed **the scope of the language of the specification clearly corresponds to the language of the claims**, the "polymerizable material" of the claims being referred to variously by the specification as a "polymer" and a "*polymerizable* mass * * * added * * * as an aqueous solution of monomeric *material*, such as hexamethylenediamine adipate." (Emphasis supplied.)* Thus there is no basis for the solicitor's reliance upon the description requirement as support for the rejection here.

Bowen:[35]

The Federal Circuit confirmed that written description can be satisfied with any one of various different methods:

> Depending upon the facts of each particular case, one may satisfy the written description requirement using, for example, drawings, **tables**, equations, and formulas, **alone** or in combination.

Hunter.[36] The Federal Circuit in Union Oil[37] uses a simple tabular method to illustrate written description.

According to the Deputy Assistant Commissioner for Patent Policy and Projects,[38] electrical applications with detailed drawings meet the written description requirement:

> [I]n most applications which include detailed drawings, e.g., most mechanical and electrical applications, the examiner will be able to quickly determine that the written description requirement has been met.

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35. In re Bowen, 492 F.2d 859, 181 USPQ 48, 52 (CCPA 1974) (emphasis added).

36. In re Hunter, No. 94-1301, 1995 U.S. App. LEXIS 15363, at *14 (Fed. Cir. June 19, 1995) (emphasis added).

37. Union Oil Co. of California v. Atlantic Richfield, 208 F.3d 989, 54 USPQ2d 1227 (Fed. Cir. 2000).

38. Stephen G. Kunin, "Written Description Guidelines and Utility Guidelines," Journal of the Patent and Trademark Office Society (JPTOS), Vol. 82, No. 2 at page 87 (February 2000).

In further support of the above, it is black-letter law that an original claim is its own written description. Hence, written description needs no more detail than the claim limitations. See Purdue and Bowen above.

> Where the claim is an original claim, the underlying concept of insuring disclosure as of the filing date is satisfied, and the description requirement has likewise been held to be satisfied.

Smith.[39]

> Claim 2, which apparently was an original claim, in itself constituted a description in the original disclosure equivalent in scope and identical in language to the total subject matter now being claimed. See In re Anderson, 471 F.2d 1237, 176 USPQ 331 (CCPA 1973). Nothing more is necessary for compliance with the description requirement of the first paragraph of 35 U.S.C. 112.

Gardner.[40]

Similarly, the ITC held that disputed "claim language" found in an original claim satisfies written description. The ITC also held that original claims can be considered in "part":

> The ALJ found claim 9 of the `838 patent invalid under 35 U.S.C. § 112 as not meeting the written description and claim precision requirements because claim 9 calls for "jaws which grip the fastener at opposite ends," but the specification and drawings show gripping at one end. Since **the claim language questioned is part** of original claim 9, it is its own description, and there is no failure to meet the written description requirement. We also find that claim 9 is not indefinite.

Plastic Fastners.[41]

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39. In re Smith, 481 F.2d 910, 178 USPQ 620, 624 (CCPA 1973).

40. In re Gardner, 475 F.2d 1389, 177 USPQ 396, 397 (CCPA 1973).

41. In re Certain Plastic Fasteners and Processes for the Manufacture Thereof, 1987 ITC Lexis 271 (on Petition For Review) (emphasis added).

It is also black-letter law that a claim defines the "boundary" of the claimed invention and is not a detailed technical description.

> The purpose of claims is not to explain the technology or how it works, but to state the legal boundaries of the patent grant.

S3 Inc.[42]

> A claim is a group of words defining only the boundary of the patent [property].

Buehler.[43]

> A claim is a group of words defining only the boundary of the patent monopoly. It may not describe any physical thing and indeed may encompass physical things not yet dreamed of.

Vogel.[44]

> Distinguishing what infringes from what doesn't is the role of the claims....

Gore.[45]

Hence, because an original claim is its own written description and because a claim defines a "boundary" of an invention, written description requires no more.

Despite the fact that written description does not require any more than antecedent basis for the claim limitations (e.g., an original claim is its own written description), written description does not even require disclosure of the same words as

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42. See S3 Inc. v. nVIDIA Corp., 259 F.3d 1364, 59 USPQ2d 1745, 1748 (Fed. Cir. 2001).

43. In re Buehler, 515 F.2d 1134, 185 USPQ 781, 787 (CCPA 1975).

44. In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

45. W. L. Gore & Associates, Inc., v. Garlock, Inc., 721 F.2d 1540, 1557 (Fed. Cir. 1983).

the claim limitations -- it is adequate for the antecedent basis to be express, implicit, or inherent in the disclosure.

> While there is no in haec verba requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure.

PTO Guidelines at Section I.B.[46]

> **2163.02 Standard for Determining Compliance With the Written Description Requirement** * * *
> The subject matter of the claim need not be described literally (i.e., using the same terms or in haec verba) in order for the disclosure to satisfy the description requirement.

MPEP 2163.02.

> Where the language of the claims is descriptively supported either in a drawing or, for example, as the cumulative effect of numerous specific embodiments described in the application, it is not necessary that the specific language used as a definition in the claim also be used in the specification as originally filed.

Kayton.[47]

> The function of the description requirement is to ensure that the inventor had possession of, as of the filing date of the application relied upon, the specific subject matter later claimed by him; **how the specification accomplishes this is not material**. In re Smith, 481 F.2d 910, 178 USPQ 620 (CCPA 1973). The claimed subject matter need not be described in haec verba to satisfy the description requirement. In re Smith, 59 CCPA 1025, 458 F.2d 1389, 173 USPQ 679 (CCPA 1972). It is not necessary that the application describe **the claim limitations** exactly, but only so clearly that one having ordinary skill in the pertinent art would recognize from the disclosure that appellants invented processes including **those limitations**. In re Smythe, 480 F.2d 1376, 178 USPQ 279 (CCPA 1973).

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46. Guidelines for the Examination of Patent Applications Under the 35 U.S.C. 112, ¶ 1, "Written Description" Requirement; Official Gazette 1242 O.G. 168 (January 30, 2001).

47. Kayton, I., Patent Practice, Fifth Edition, Vol. 3, Chapter 11, page 92 (Patent Resources Institute, 1993).

Herschler.[48] Notwithstanding the fact that the disclosure has extensive support for the claimed invention, such support is not even required for written description:

> Compliance with the written description requirement of Section 112 only requires that appellant's application contain sufficient disclosure, **expressly or inherently**, to make it clear to persons skilled in the art that appellant possessed the subject matter claimed. In re Mott, 539 F.2d 1291, 190 USPQ 536, 541 (CCPA 1976). The test for determining compliance with the written description requirement is whether the disclosure of the application as originally filed **reasonably** conveys to the artisan that the inventor had possession of **the claimed subject matter**, rather than the presence or absence of literal support in the specification for the claim language. In re Kaslow, 707 F.2d 1366, 217 USPQ 1089, 1096 (Fed. Cir. 1983).

Harvey.[49]

The Federal Circuit in Union Oil[50] cited to Vas-Cath with approval stating (emphasis added):

> However, neither the Patent Act nor the case law of this court requires such detailed disclosure. *See ... Vas-Cath*, 935 F.2d at 1566 ("ranges found in applicant's claims need not correspond exactly to those disclosed in [the specification]; **issue is whether one skilled in the art could derive the claimed ranges from the [] disclosure**.")

The court then quoted this Vas-Cath statement yet a second time. See Union Oil at 1235.

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48. In re Herschler, 591 F.2d 693, 700-01, 200 USPQ 711, 717 (CCPA 1979) (emphasis added).

49. Ex Parte Harvey, 3 USPQ2d 1626, 1627 (Bd. Pat. App. and Int. 1986) (emphasis added).

50. Union Oil Co. of California v. Atlantic Richfield, 208 F.3d 989, 54 USPQ2d 1227, 1233 (Fed. Cir. 2000).

Judge Stewart in Hyatt-'211[51] (emphasis added) stated:

> We have considered, in detail, the language objected to by the examiner, but find the language to be **reasonably descriptive** of the invention.... Accordingly, we will not sustain the rejection.

Thus, the written description requirement must be reasonably applied.

The PTO Guidelines[52] confirm the relevance of reduction-to-practice to written description:

> Possession may be shown in a variety of ways including description of an actual reduction to practice ....

However, the rejections do not properly address the disclosed actually reduced-to-practice "Experimental System". When the Applicant has gone through all of the effort and expense to actually reduce-to-practice and to disclose in detail an embodiment, the Examiner is required to consider this very compelling evidence. The Examiner must consider the disclosure as a whole "taking into account evidence that ... detracts from an agency's decision".

> The [U.S. Supreme] Court has emphasized that "substantial evidence" review involves examination of the record as a whole, taking into account evidence that both justifies and detracts from an agency's decision. See Universal Camera Corp. v. NLRB, 340 U.S. 474, 487-88 (1951).

Gartside.[53]

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51. Ex parte Hyatt, Appeal No. 91-2061, Paper No. 28 at 9 in patent application Serial No. 07/662,211 (PTO Bd. App. December 20, 1991) [herein Hyatt-'211] (unpublished PTO decision).

52. Guidelines for Examination of Patent Applications Under the 35 USC 112, § 1, `Written Description' Requirement; Official Gazette at 1242 OG 168, 172 (January 30, 2001).

53. In re Gartside, 53 USPQ2d 1769, 1773 (Fed. Cir. 2000).

In summary, the written description requirement is "relatively simple to comply with and thus will ordinarily demand minimal concern on the part of the Patent Office".

1.11 The Federal Circuit Analyzes Written Description On An Individual Limitation-By-Limitation Basis In Simple Tabular Form

The Federal Circuit analyzes written description on an individual claim limitation by claim limitation basis in a simple tabular form (see table below). See Union Oil.[54] See also Hunter:[55]

> Depending upon the facts of each particular case, one may satisfy the written description requirement using, for example, drawings, **tables**, equations, and formulas, **alone** or in combination.

This tabular form was generated by the court in Union Oil:

> To reiterate, this court supplies the written description supporting another claim, claim 125 as follows:

What follows this statement is another table of the type shown below.

The Federal Circuit even cites to an important limitation from an original claim and combines it with other limitations excerpted from the body of the patent (see table below). It is particularly noteworthy that this original claim was previously canceled and is not in the patent.[56]

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54. Union Oil Co. of California v. Atlantic Richfield, 208 F.3d 989, 54 USPQ2d 1227, 1233 (Fed. Cir. 2000).

55. In re Hunter, No. 94-1301, 1995 U.S. App. LEXIS 15363, at *14 (Fed. Cir. June 19, 1995) (emphasis added).

56. This may be considered to be the intermixing of citations to two separate documents, the original application containing the original claim and the patent to which the other citations are made.

The instant disclosure has hundreds of occurrences of claim limitations and has extensive enabling disclosures of these claim limitations. This is far more than the tables in Union Oil citing to a single recitation in the disclosure for each claim limitation.

Claim limitation	Support in '393 patent
T50 at ≤ 200°	Col. 14, ll. 9-15: "no greater than 210° F., . . . *but preferably less than 210° F.* . . ."
RVP at ≤ 7.0 psi	Col. 14, ll. 36-40: "Reid Vapor Pressure specification of 8.0 psi . . . *even more preferably no greater than 7.0 psi* . . ."
Olefin at < 4.0 volume percent	Col. 14, ll. 23-30: "varying the olefin content, this value is generally maintained less than 15 volume percent, with decreasing values providing progressively improved results. Thus, it is contemplated that each unit reduction, e.g., to values *below* . . . *4* . . . *providing progressively better results.* . . . "
Paraffin at > 85 volume percnet [sic]	Col. 14, ll. 49-64: "progressively increasing the paraffin content progressively decreases the CO emitted. Accordingly . . . the paraffin content would be increased to . . . and *most preferably of all above 85 volume percent.* . . ."
T90 at ≤ 300°	claimed exactly in original claim 29
T10 at ≤ 158°	Col. 5, lls. 6-30: Table 1 shows maximum T10 distillation temperatures for all five volatility classes at *158 or below.*

Union Oil at 1233 (footnote omitted).

As discussed above, the Federal Circuit confirmed that written description can be satisfied with a table "**alone**":

> Depending upon the facts of each particular case, one may satisfy the written description requirement using, for

example, drawings, **tables**, equations, and formulas, **alone** or in combination.

Hunter.[57] The Federal Circuit in Union Oil uses a simple tabular method to illustrate written description (see above).

1.12 The Claims More Than Satisfy The Law On Enablement

It is black-letter law that the test for enablement is whether there is "undue experimentation" and it is black-letter law that the disclosure can rely on the skill in the art.

> The test of enablement is whether one reasonably skilled in the art could make or use the Invention from the disclosures in the patent coupled with information known in the art without undue experimentation.

US v. Telectronics.[58]

The U.S. Supreme Court requires the Examiner to treat knowledge which is common and well known as if it were written out in the patent and delineated in the drawings:

> He [an engineer] may begin at the point where his invention begins, and describe what he has made that is new, and what it replaces of the old. **That which is common and well known is as if it were written out in the patent and delineated in the drawings.**

Loom.[59] The Federal Circuit reiterates the law of the U.S. Supreme Court:

> Paragraph 1 permits resort to material outside of the specification in order to satisfy the enablement portion of the statute because **it makes no sense to encumber the**

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57. In re Hunter, No. 94-1301, 1995 U.S. App. LEXIS 15363, at *14 (Fed. Cir. June 19, 1995) (emphasis added).

58. United States v. Telectronics, Inc., 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988).

59. Loom Co. v. Higgins, 105 U.S. 580, 585 (1881) (emphasis added).

> **specification of a patent with all the knowledge of the past concerning how to make and use the claimed invention**. One skilled in the art knows how to make and use a bolt, a wheel, a gear, a transistor, or a known chemical starting material. The specification would be of enormous and unnecessary length if one had to literally reinvent and describe the wheel.

Atmel.[60]

The Federal Circuit requires the Examiner to consider the disclosure as a whole in order to evaluate enablement.

> Thus, the examiner and the board effectively ignored statement [D] and the rest of the disclosure. This was error because the specification disclosure *as a whole* must be considered. *In re Moore, supra.*
>
> The PTO not having carried its burden of establishing lack of enablement, this rejection of claim 14 under § 112, first paragraph, is reversed.

Hogan.[61] However, the Examiner has not considered the disclosure as a whole.

1.13 The Extensively Disclosed Actually Reduced-To-Practice "Experimental System"

The Abstract prominently identifies the "experimental system" and states that it "is disclosed in detail" (emphasis added).

> ABSTRACT
>
> An improved image processing architecture is provided having advantages of increased speed, lower cost, extensive features and efficiency of implementation.... An **experimental system** that demonstrates many of the improved features has been constructed and is **disclosed in detail**.

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60. Atmel Corp. v. Info. Storage Devices, Inc., 198 F.3d 1374, 53 USPQ2d 1225, 1230 (Fed. Cir. 1999) (emphasis added).

61. In re Hogan, 559 F.2d 595, 194 USPQ 527, 539 (CCPA 1977).

The disclosure has **more than 40 recitations** of the term experimental system and terms related thereto.

The disclosure has **more than 30 sheets of figures** directed to the actually reduced-to-practice "Experimental System" (e.g., Figs. 6A-6AH).

The disclosure has **more than 200 pages of description** directed to the actually reduced-to-practice "Experimental System" (e.g., Spec. at 240-373 and 503-574).

The disclosure titles prominently emphasize the actually reduced-to-practice "Experimental System".

TABLE OF CONTENTS

LIST OF TABLES

The application even discloses cable lists and IC DIP component layout on circuit boards (Spec. at 510-543).

The hardware and software of the actually reduced-to-practice "Experimental System" is summarized in the disclosure.

EXPERIMENTAL CONFIGURATION FEATURES TABLE

- Real time operation
  - Medium resolution (260,000-pixels per frame)
  - Dynamic updates at the field rate (60-times per second)
- Interactive operation
  - Joysticks and computer commands
    - X-axis translation
    - Y-axis translation
    - Rotation
    - Expansion and compression
  - Instantaneous response
  - Simultaneous motion, all controls
- Geometric processing
  - Rotation
    - Continuous
    - Resolution: 0.2-degrees
    - 360-degrees/sec max rate
      - Software limited
      - Expandable

Translation
Continuous
Resolution: 1-pixel
1000-pixels/second max rate
Software limited
Expandable
Expansion/compression
Continuous
Fractional (non-integer)
Resolution: 1-pixel
Double/half size per second max rate
Software stops
Expandable
Monitor
Barco color monitor.
Blanked to 484-lines and about 700-pixels/line
3-colors, RGB
13-inch CRT
Inline gun shadow mask
Image memory
512-pixels by 512-pixels
7-bits per pixel
2-bits red
2-bits blue
3-bits green
200-ns RAMs
Spatial filtering
9-pixel kernel at 10-million kernels/sec
Weight RAM
Virtual scrolling
Image memory wrap-around
Supervisory computer
8085 8-bit microcomputer
CP/M-80 operating system
Compiled Basic

Spec. at 33.

Many other disclosure sections and the figures discussed therein teach features of the actually reduced-to-practice "Experimental System". For example, the following sections supplement the above table of contents quotations with theory, analysis, and documentation related to the disclosed actually reduced-to-practice "Experimental System".

TABLE OF CONTENTS

* * *

LIST OF TABLES

1.14 The Examiner Has Not Established That Any Experimentation Would Be Required In View Of The Actually Reduced-To-Practice "Experimental System"

1.14.1 Introduction

Enablement is established, as here, when there is **no** "undue experimentation".

> The test of enablement is whether one reasonably skilled in the art could make or use the Invention from the disclosures in the patent coupled with information known in the art without undue experimentation.

Telectronics.[62] The PTO confirms that "experimentation" is the standard for enablement. MPEP 2164.01.

> The standard for determining whether the specification meets the enablement requirement was cast in the Supreme Court decision of *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916) which postured the question: is the experimentation needed to practice the invention undue or unreasonable? That standard is still the one to be applied. *In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988). Accordingly, even though the statute does not use the term "undue experimentation." It has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. *In re Wands*, 858 F.2d at 737, 8 USPQ2d at 1404 (Fed. Cir. 1988). *See also United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988) ("The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation.")

Hence, if there is **no** undue experimentation, enablement is established.

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62. United States v. Telectronics, Inc., 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988).

The nature of experimentation is articulated in Norwest, WICOR, and United Stationers,[63] as discussed below. Simply stated, experimentation involves technical uncertainty about the possibility of developing a system from the start of the project (the filing of the ancestor application). These authorities establish that software development is routine and does not involve experimentation unless it satisfies certain legal requirements. However, in the present case, where an artisan is starting with the disclosed actually reduced-to-practice "Experimental System" and other disclosures, where the rejection does not address uncertainty in making or using the invention, there should be no experimentation and certainly not undue experimentation.

The established test for experimentation is technical "uncertainty from the outset". Simply stated, this means technical uncertainty about the possibility of developing the product from the start of the project. In this case, the start of the project is the instant disclosure including the disclosed actually reduced-to-practice "Experimental System".

The issue here is whether an artisan; starting with the disclosed actually reduced-to-practice "Experimental System", the additional disclosure in the instant application, and the skill in the art; would be enabled to make and use the claimed invention. This starting point is the "outset". The test is whether an artisan making and using the claimed invention in this environment would be "uncertain at the outset."

The conclusion must be that, "at the outset", it was not uncertain that an artisan would be enabled to make and use the claimed invention. Starting with the disclosed actually reduced-

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63. Norwest Corporation and Subsidiaries v. Commissioner of Internal Revenue, 110 TC 454, 507-508 (1998); WICOR, Inc., and Subsidiaries v. United States, 116 F. Supp. 2d 1028, 1035-36 (E.D. Wis. 2000); United Stationers, Inc. v. United States, 163 F.3d 440, 445-46 (7th Cir. 1998).

to-practice "Experimental System", the additional disclosures in the instant application, and the skill in the art; an artisan would have been enabled to make and use the claimed invention.

1.14.2 The Established Law On Experimentation

The established law on the nature of experimentation is articulated by Norwest, WICOR, and United Stationers[64] -- technical uncertainty about the possibility of developing the product from its outset.

The court in WICOR stated:

> The government responds that the WICOR project did not involve developing a new computer system in which the design was uncertain at the outset.
>
> The plaintiff failed to present evidence that the means for achieving the final result of the WICOR project were uncertain at the outset.

116 F. Supp. 2d at 1035.

> The plaintiff failed to present evidence that the means for achieving the final result of the WICOR project were uncertain at the outset. For example, Paul Kowalski, the WICOR credit team leader, testified that the WICOR project team followed a tried and true data processing approach -- the DB-2 system. Perhaps most telling is Kowalski's acknowledgment that the data processing system utilized by WICOR was not new, although it was new to WICOR (Kowalski Dep. at pp. 28-29). However, a method does not constitute a process of experimentation simply because the method is experimental to a specific taxpayer. Rather, the method must be experimental to the relevant field -- in this case, computer science. Kowalski's testimony belies the plaintiff's assertion that the WICOR project was experimental to the field of computer science.

116 F. Supp. 2d at 1035-36.

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64. Norwest Corporation and Subsidiaries v. Commissioner of Internal Revenue, 110 TC 454, 507-508 (1998); WICOR, Inc., and Subsidiaries v. United States, 116 F. Supp. 2d 1028, 1035-36 (E.D. Wis. 2000); United Stationers, Inc. v. United States, 163 F.3d 440, 445-46 (7th Cir. 1998).

> The court is persuaded by the testimony offered by the government's experts -- Dr. Srivastava and Thomas Niccum -- that the project did not involve identification of models or theories of computer science using a process of experimentation and that there was not a systematic research-oriented process by which data was collected for analysis of competing hypotheses. Although WICOR developed "lessons learned" reports, these reports were informal and only identified miscellaneous programming errors. The court concludes that the WICOR project did not constitute a process of experimentation.

116 F. Supp. 2d at 1036.

> According to USI's dictionary, an experiment is "... a test, trial, or tentative procedure, an act or operation for the purpose of discovering something unknown or of testing a principle, supposition, etc." Appellant's Br. at 23 (citing Random House College Dictionary 465 (rev. ed. 1984)).

163 F.3d at 445 (alteration in original).

> The legislative history of § 41(d)(1)(C) bolsters this conclusion. The Conference Report explains the meaning of the process of experimentation test: The term process of experimentation means a process involving the evaluation of more than one alternative designed to achieve a result where the means of achieving that result is uncertain at the outset. This may involve developing one or more hypotheses, testing and analyzing those hypotheses (through, for example, modeling or simulation), and refining and discarding the hypotheses as part of a sequential design process to develop the overall component.
>
> Thus, for example, costs of developing a new or improved business component are not eligible for the credit if the method of reaching the desired objective (the new or improved product characteristics) is readily discernible and applicable as of the beginning of the research activities, so that true experimentation in the scientific or laboratory sense would not have to be undertaken to develop, test, and choose among viable alternatives . . . . Engineers who design a new computer system, or who design improved or new integrated circuits for use in computer or other electronic products, are engaged in qualified research because the design of those items is uncertain at the outset and can only be determined through a process of experimentation relating to specific design hypotheses and decisions as described above.

163 F.3d at 445-46 (alteration in original).

> H.R. Conf. Rep. No. 99-841, at II-72 (1986).... The Report suggests that qualifying research must from its outset involve some technical uncertainty about the possibility of developing the product. See *Norwest, 1998 U.S. Tax Ct. LEXIS 32, P 52,758, at 4655* (discussing the "required uncertainty"); cf. *TSR, 96 T.C. at 920-21.*

163 F.3d at 446.

> None of the summaries, however, describes any technical uncertainty about actually developing the programs. Compare *Norwest, 1998 U.S. Tax Ct. LEXIS 32, P 52,758, at 4670* (programming project did not constitute qualified research because, in part, it did not involve technical risk). Nor were there any doubts about the ability of computers to perform the invoicing, billing and marketing tasks. That is, there was simply no technical uncertainty from the outset. We therefore conclude that USI's development of the eight programs did not involve a process of experimentation and that the district court did not clearly err in concluding that the projects did not involve the level of uncertainty necessary to clear this hurdle.

163 F.3d at 446.

> D. THE PROCESS OF EXPERIMENTATION TEST
>
> The process of experimentation test requires that substantially all of the activities which constitute elements of a process of experimentation relate to a new or improved function, performance, reliability, or quality. The process of experimentation test, which is referenced in the discovery test, is explained by Congress as follows:
>
> The term process of experimentation means a process involving the evaluation of more than one alternative designed to achieve a result where the means of achieving that result is uncertain at the outset. This may involve developing one or more hypotheses, testing and analyzing those hypotheses (through, for example, modeling or simulation), and refining or discarding the hypotheses as part of a sequential design process to develop the overall component.

110 T.C. at 495-96.

> Thus, for example, costs of developing a new or improved business component are not eligible for the credit if the method of reaching the desired objective (the

new or improved product characteristics) is readily discernible and applicable as of the beginning of the research activities, so that true experimentation in the scientific or laboratory sense would not have to be undertaken to develop, test, and choose among the viable alternatives.

110 T.C. at 496.

Unlike the regulations under section 174, which are silent about the means of discovering information, the conference report accompanying the TRA 1986 made it clear that a more structured method of discovery is required with respect to section 41. By requiring that at the outset uncertainty exist about the ability to develop the product in the scientific or laboratory sense, the process of experimentation test is aimed at eliminating uncertainty about the TECHNICAL ability to develop the product -- as opposed to uncertainty as to whether the product can be developed within certain business or economic constraints, even though the taxpayer knew that it was technically possible to develop it.

110 T.C. at 496.

As evidence of the required uncertainty, Congress mandated the evaluation of more than one alternative, which in turn may require the use of a structured process of experimentation through the continuous development of hypotheses that require testing and analysis until the method for reaching the objective is discovered. Congress did not specify that any particular number of hypotheses be developed by the taxpayer, but the more hypotheses that are developed, tested, and analyzed, the more likely the project will satisfy the process of experimentation test.

110 T.C. at 496.

This test also requires that "substantially all" of the activities constitute elements of a process of experimentation. This requirement raises two questions: (1) What does the term "substantially all" mean? and (2) what activities come within the elements of a process of experimentation? ....

We agree with respondent and hold that in the context of section 41, the term "substantially all" refers to at least 80 percent of the activities that constitute elements of a process of experimentation. This interpretation is consistent with the existing definition of "substantially all" in the regulations under section 41 with respect to qualified wages.

110 T.C. at 497.

> Congress indicated in the conference report accompanying the TRA 1986 those elements which constitute a process of experimentation. They include the developing, testing, and analyzing of hypotheses. They do not include activities performed after commercial production or implementation or otherwise set forth in section 41(d)(4). See H. Conf. Rept. 99-841 (Vol. II), supra at II- 72, *1986-3 C.B. (Vol. 4) at 72*. However, in the case of internal use software, exceptions are made for the modifications of commercially available software. See infra.
>
> Thus, at least 80 percent of the activities engaged in by a taxpayer with respect to the preproduction or implementation development of a product must involve the development, testing, and analysis of hypotheses that are designed to eliminate technical uncertainty as to the development of that product. This then raises the issue of which activities in a project are to be examined together and which are to be examined separately for purposes of section 41.

110 T.C. at 497.

> In that regard, the court found that the taxpayer did not expand or refine existing principles of computer science, stating: "Rather, Stationers merely applied, modified, and at most, built upon, pre-existing, technological information already supplied to it. This is a far-cry from what Congress contemplated when it spoke of research directed at the 'principles of computer science'." *982 F.Supp. at 1284*.

110 T.C. at 502.

1.14.3 The Electronics And Programming Arts Are Very Predictable

It is black-letter law that the electronics and programming arts are very predictable as of the effective filing date. See the law cited below.

> As we explained in *In re Fisher*, 57 CCPA at 1108, 427 F.2d at 839, 166 USPQ at 24:
>
> **In cases involving predictable factors, such as mechanical or electrical elements**, a single embodiment

provides broad enablement in the sense that, **once imagined**, other embodiments can be made **without difficulty** and their performance characteristics **predicted** by resort to known scientific laws. In cases involving unpredictable factors, such as most chemical reactions and physiological activity, the scope of enablement obviously varies inversely with the degree of unpredictability of the factors involved.

Bowen.[65] See also Fisher.[66]

Further with respect to the prima facie case of non-enablement, we note that a single embodiment may provide broad enablement **in cases involving predictable factors, such as mechanical or electrical elements**.

Hitzemann.[67]

The scope of the required enablement varies inversely with the degree of predictability involved, but even in unpredictable arts, a disclosure of every operable species is not required. A single embodiment may provide broad enablement **in cases involving predictable factors, such as mechanical or electrical elements**. *In re Vickers*, 141 F.2d 522, 526-27, 61 USPQ 122, 127 (CCPA 1944); *In re Cook*, 439 F.2d 730, 734, 169 USPQ 298, 301 (CCPA 1971).

MPEP 2164.03 (emphasis added).

The PTO presents its definition for "predictability" in MPEP 2164.03.

The "predictability or lack thereof" in the art refers to the ability of one skilled in the art to extrapolate the disclosed or known results to the claimed invention. If one skilled in the art can readily anticipate the effect of a change within the subject matter to which the claimed invention pertains, then there is predictability in the art.

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65. In re Bowen, 492 F.2d 859, 181 USPQ 48, 50 (CCPA 1974) (emphasis added).

66. In re Fisher, 427 F.2d 833. 166 USPQ 18, 24 (CCPA 1970).

67. Ex parte Hitzeman, 9 USPQ2d 1821, 1823 (Bd. Pat. App. & Int. 1988) (emphasis added).

It is well established that the electronic art is highly predictable (discussed below).

The electrical art is predictable (MPEP 2164.03).

> Where, as here, a claimed genus represents a diverse and relatively poorly understood group of microorganisms, the required level of disclosure will be greater than, for example, the disclosure of an invention involving a "predictable" factor such as a mechanical or electrical element.

Vaeck.[68]

The programming art is as predictable as the electrical art:

> "[it is a] fundamental and well understood tenet of the computing art [that] ... '**[a]ny software process can be transformed into an equivalent hardware process, and any hardware process can be transformed into an equivalent software process**.'" *See* Ed Klingler [sic, Klingman], *Microprocessor Systems Design* 5 (1977). Dr. Rhyne stated that this "dualistic transformation," known as the "hardware-/software" tradeoff, effectively means that the selection of a software pointer for a microprocessor versus a hardware switch to control a microprocessor-based system is simply a matter of design choice. This record evidence shows that one of skill in the art would recognize these alternative systems as interchangeable substitutes.

Overhead Door.[69]

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68. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438, 1445 (Fed. Cir. 1991).

69. Overhead Door v. Chamberlain, 194 F.3d 1261, 52 USPQ2d 1321, 1326 (Fed. Cir. 1999) (emphasis added).

1.14.4 Routine Software Development Does Not Involve Experimentation Even Without Considering The Actually Reduced-To-Practice "Experimental System"

"[R]outine software development" does not involve experimentation. This is particularly compelling in view of the disclosed actually reduced-to-practice "Experimental System" and other disclosures and the predictability of the programming art.

The U.S. Supreme Court set the stage in Loom:[70]

> The specification ... proceeds to describe the mechanism of the invention by a description and reference to drawings ... all which would be incomprehensible to a person unacquainted with looms for weaving pile fabrics, but very plain to one who understood their construction and operation at the date of the patent. A person skilled in the art of constructing or using such looms ... would readily appreciate the meaning of the terms and the character of the improvement described....
>
> When an astronomer reports that a comet is to be seen with the telescope in the constellation of Auriga, in so many hours and minutes of right ascension, it is all Greek to the unskilled in science; but other astronomers will instantly direct their telescopes to the very point in the heavens where the stranger has made his entrance into our system. They understand the language of their brother scientist. If a mechanical engineer invents an improvement on any of the appendages of a steam engine ... he is not obliged, in order to make himself understood, to describe the engine, nor the particular appendage to which the improvement refers, nor its mode of connection with the principle machine. These are already familiar to others skilled in that kind of machinery. He may begin at the point where his invention begins, and describe what he has made that is new, and what it replaces of the old. **That which is common and well known is as if it were written out in the patent and delineated in the drawings.**

Similarly, because computer program knowledge "is common and well known [it] is as if it were written out in the patent and delineated in the drawings."

---

70. Loom Co. v. Higgins, 105 U.S. 580, 585 (1881) (emphasis added).

The CCPA in Sherwood then applied this century-old U.S. Supreme Court wisdom to computer programming:

> In general, writing a computer program may be a task requiring the most sublime of the inventive faculty or it may require only the droning use of a clerical skill. The difference between the two extremes lies in the creation of mathematical methodology to bridge the gap between the information one starts with (the "input") and the information that is desired (the "output"). If these bridge-gapping tools are disclosed, there would seem to be no cogent reason to require disclosure of the menial tools known to all who practice this art.

Sherwood.[71]

> In assessing any computer-related invention, it must be remembered that the programming is done in a computer language. The computer language is not a conjuration of some black art, it is simply a highly structured language. Analogously, if a person were to express a complete thought in German, it would be no trick for a translator to convert that thought into a palpable English form. The thought, thus expressed, might not be worthy of Shakespeare, but it would be understandable to one who uses the English language. Similarly, the conversion of a complete thought (as expressed in English and mathematics, i.e., the known input, the desired output, the mathematical expressions needed and the methods of using those expressions) into the language a machine understands is necessarily a mere clerical function to a skilled programmer.

Sherwood.[72]

> Taking into account the expert opinions found in the two affidavits, it would appear that the detailed disclosure of the analog method in combination with the suggestion that a digital method should be used might be more enlightening to one having ordinary skill in the art than the computer listing or flow chart required by the PTO. We view the PTO's requirement as quite formalistic in view of the verbal flow chart provided by appellant in the specification. In any event, the touchstone is the content, not its form.

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71. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544 (CCPA 1980).

72. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544 n.6 (CCPA 1980).

Sherwood.[73]

The Federal Circuit in Robotic[74] held that software does not have to be disclosed to be enabling, even undisclosed software can be enabling if it is apparent to an artisan or implicit in the disclosure.

The Federal Circuit cited to Sherwood with approval and elaborated on software disclosure regarding written description, enablement, and experimentation -- the disclosure does not need to disclose flow charts or computer source code listings, "a disclosure of the functions of the software" is adequate:

> GE argues that the patent fails to disclose two software routines....
>
> As a general rule, where software constitutes part of a best mode of carrying out an invention, description of such a best mode is satisfied by **a disclosure of the functions of the software**. This is because, normally, writing code for such software is within the skill of the art, not requiring undue experimentation, once its functions have been disclosed. It is well established that what is within the skill of the art need not be disclosed to satisfy the best mode requirement as long as that mode is described. **Stating the functions of the best mode software satisfies that description test**. We have so held previously and we so hold today. *See In re Hayes Microcomputer Prods., Inc. Patent Litigation, 982 F.2d 1527, 1537-38, 25 U.S.P.Q. 2D (BNA) 1241, 1248-49 (Fed. Cir. 1992); In re Sherwood, 613 F.2d 809, 816-17, 204 U.S.P.Q. (BNA) 537, 544 (CCPA 1980)*. Thus, **flow charts or source code listings are not a requirement for adequately disclosing the functions of software**. *See Sherwood, 613 F.2d at 816-17, 204 U.S.P.Q. (BNA) at 544*. Here, substantial evidence supports a finding that the software functions were disclosed sufficiently to satisfy the best mode requirements. See *Hayes, 982 F.2d at 1537, 25 U.S.P.Q. 2D (BNA) at 1248-49* (stating that there was no best mode violation where the specification failed to disclose a firmware listing or flow charts, but did

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73. In Re Sherwood, 613 F.2d 809, 204 USPQ 537, 544-545 n.8 (CCPA 1980).

74. Robotic Vision Systems, Inc. v. View Engineering Inc., 42 USPQ2d 1619, 1622 (Fed. Cir. 1997).

> disclose sufficient detail to allow one skilled in the art to develop a firmware listing for implementing the invention).
>
> A finding that the GMB was sufficiently disclosed to satisfy the best mode requirement was also supported by substantial evidence. Fonar's witness testified that the '966 patent provided a description of the function of the GMB with reference to the components within the dotted line in Figure 7 of the '966 patent, reproduced below.

Fonar.[75]

Similar to the CCPA's position in Sherwood (above), the Federal Circuit established that all that was needed to satisfy § 112-1 for a complex claim directed to a microprocessor-based modem was (1) identification of a commercial microprocessor and (2) a brief description of the **function** to be performed:

> Disclosing a microprocessor capable of performing certain functions is sufficient to satisfy the requirement of section 112, first paragraph, when one skilled in the relevant art would understand what is intended and know how to carry it out....
>
> The disclosure sufficiently recites **the function of the firmware**.... The evidence supports the conclusion that one of ordinary skill in the art would understand how to implement the timing means with a microprocessor without a firmware listing.... The evidence of record supports the conclusion that **all that was required for one of ordinary skill in the art to understand what the invention was and how to carry it out was the disclosure of a microprocessor having certain capabilities and the desired functions it was to perform** ....
>
> Ven-Tel also focuses on the fact that the heart of the claimed invention of the '302 patent is described only in twenty-seven lines. Certainly no length requirement exists for a disclosure to adequately describe an invention. While some inventions require more disclosure, the adequacy of the description of an invention depends n its content in relation to the particular invention, not its length.

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75. Fonar Corp. v. General Electric Co., 107 F.3d 1543, 41 USPQ2d 1801, 1804-05, (Fed. Cir. 1997) (emphasis added).

Hayes.[76]

> While we agree that the '302 patent only discloses the **general function** of the firmware without teaching mathematical formulas, flow charts, or a firmware program listing, **no more was needed here**.

Hayes.[77] The instant disclosure describes "the desired functions it was to perform" in significantly more detail than the 27 line description of the Hayes patent and the instant disclosure expressly teaches a dual 8085-8088 microprocessor arrangement in a commercial CompuPro computer system product:

> The computer is implemented with various S-100 boards manufactured by CompuPro including the 8085-8088 CPU board, RAM 16 and RAM 17 memory boards, a System Support board, and a pair of Interfacer 2 boards.... These boards are described in detail in the referenced manuals.

Spec. at 297.

The Federal Circuit in Union Oil[78] cited to Hayes and Vas-Cath with approval stating:

> Appellant refiners assert that the specification does not describe the exact chemical component of each combination that falls within the range claims of the '393 patent. However, neither the Patent Act nor the case law of this court requires such detailed disclosure. *See In re Hayes Microcomputer Prods., Inc. Patent Litigation*, 982 F.2d 1527, 1533, 25 USPQ2d 1241, 1245 ("[The applicant] does not have to describe exactly the subject matter claimed."); *Vas-Cath*, 935 F.2d at 1566 ("ranges found in applicant's claims need not correspond exactly to those disclosed in [the specification]; issue is whether one skilled in the art could derive the claimed ranges from

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76. In re Hayes Microcomputer Products Inc., 982 F.2d 1527, 25 USPQ2d 1241, 1246 (Fed. Cir. 1992) (footnote omitted, emphasis added).

77. In re Hayes Microcomputer Products Inc., 982 F.2d 1527, 25 USPQ2d 1241, 1248 (Fed. Cir. 1992) (emphasis added).

78. Union Oil Co. of California v. Atlantic Richfield, 208 F.3d 989, 54 USPQ2d 1227, 1233 (Fed. Cir. 2000).

> the [] disclosure.") Rather, the Patent Act and this court's case law require only sufficient description to show one of skill in the refining art that the inventor possessed the claimed invention at the time of filing.

This statement has even greater relevance to the instant case because the Federal Circuit confirmed that, even in the **relatively unpredictable** chemical art, a disclosure does not have to describe the exact chemical components of a claim combination. Yet the instant claimed invention is in the **highly predictable** electrical and programming arts and the instant disclosure does describe claim limitations exactly. Because the unexact chemical disclosure in Union Oil was sufficient for that unpredictable art, then the exact disclosures in the instant application are certainly more than sufficient for the highly predictable electrical and programming arts. This notwithstanding the disclosed actually reduced-to-practice "Experimental System" and the significant other disclosures.

The Federal Circuit in Northern Telecom[79] then further applied the century-old U.S. Supreme Court wisdom (Loom) to computer programming:

> Further, experts for both sides testified that an experienced programmer could, without unreasonable effort, write a program to carry out the invention of the `375 patent.
>
> * * *
>
> The great weight of the expert testimony on both sides was that a programmer of reasonable skill could write a satisfactory program with ordinary effort. This requires the conclusion that the programs here involved were, to a skilled programmer, **routine**.

---

79. Northern Telecom Inc. v. Datapoint Corp., 908 F.2d 931, 15 USPQ2d 1321, 1329-1330, (Fed. Cir. 1990), cert. denied, 498 U.S. 970 (emphasis added).

The instant disclosure even provides source code for computer programs.

Table of Contents.

Very recently other courts -- Norwest, WICOR, and United Stationers discussed above -- further refine this century-old U.S. Supreme Court wisdom for computer programming:

> Dr. Walter Scacchi [plaintiff's expert] distinguished the engineering method from the scientific, empirical, and analytical methods of experimentation.

116 F. Supp. 2d at 1035.

Experimentation involves more than simply debugging a computer program:

> The projects fit squarely within this definition, USI claims, because software development involves debugging, a process of testing and correcting computer programs. We find this argument unpersuasive. Debugging programs amounts simply to fine-tuning computer operating instructions. Although we are reluctant to establish bright-line rules -- § 41 cases will always be highly fact-intensive -- we think that a process of experimentation involves something more than simply debugging a computer program. See *Norwest, 1998 U.S. Tax. Ct. LEXIS 32, P 52,758, at 4669* (computer programming project did not qualify because it "merely required conducting good coding and eliminating bugs through testing").

United Stationers at 445.

The court in Norwest stated:

> It is my [Dr. Davis'] opinion based on the sources provided * * * that the work performed by Norwest involved normal and routine software development. The software produced, in terms of the products and services provided, and the technology used to support it, was all within the then current state of the art in the industrial work of

management information systems. None of the documents provided suggest that any of the software developed by Norwest was, among other things, innovative or involved a significant degree of technical risk....

110 T.C. at 507 (second alteration in original).

Dr. Davis described five types of projects associated with software development: (1) Design and implementation (the de novo creation of a body of software); (2) installation and testing (the purchase and installation of software from a vendor); (3) maintenance (ongoing adjustments to the code); (4) enhancement (adding of functionality to the program); and (5) research (attempting to do something for the first time)....

110 T.C. at 507.

Dr. Davis stated that routine software development must be distinguished from software research efforts. He contended that software research is characterized by the search for information (as opposed to the production of code) n46 [FN 46: Dr. Davis dismissed Norwest's activities as not qualified research because Norwest produced operational software and not information about principles.] ....

110 T.C. at 507.

1.14.5 The Federal Circuit Held That Software Does Not Have To Be Disclosed To Be Enabling, Even Undisclosed Software Can Be Enabling If It Is Apparent Or Implicit In The Disclosure

The Federal Circuit in Robotic[80] held that software does not have to be disclosed to be enabling, even undisclosed software can be enabling if it is apparent to an artisan or implicit in the disclosure. In fact, in Robotic the Federal Circuit held that "software" did not even have to be mentioned to provide an enabling best mode:

> [2] On the other hand, the inventors in this case disclosed a device for carrying out their method, and it is plainly apparent that a computer, operating under software control, is to be interfaced to the device for controlling the movement of the sensor. Something must be connected to the device for providing control signals to the motors and for receiving information from the linear encoders concerning a position of the sensor, and there is no dispute that that something is a computer.
>
> The facts support the conclusion that software is to be used.
>
> * * *
>
> It simply states that a software program was the only means contemplated of carrying out the invention. From the record before us, it is clear that a software program was involved in the carrying out of the invention and that no other mode existed.
>
> Moreover, as asserted by Robotic, it would have been apparent to one skilled in the art, knowing that software was used in the prior art system, to use software for implementing the improved scanning method claimed in the patent. Yonescu averred that: "A person of ordinary skill in the art to which the `227 patent pertains would know and understand that software is needed to perform the patented method. The details of such software would also be within the skill of a person of ordinary skill in the art to which the `227 patent pertains." View has not provided a basis for concluding that Yonescu's assertions are not correct. Thus, one cannot conclude that a person skilled in the art would not have known that software was the best mode of carrying out the invention and how to

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80. Robotic Vision Systems, Inc. v. View Engineering Inc., 42 USPQ2d 1619, 1622 (Fed. Cir. 1997).

> implement it. The patent cannot be held to fail to comply with the best mode requirement for lack of the word "software," the use of which was plainly apparent to one skilled in the art. Such a disclosure was implicit in the specification.
>
> Finally, it has not been shown that there is a genuine issue as to whether one skilled in the art would have known how to create specific source code for this purpose. We have previously held in *Hayes* and in *Fonar* (after the district court decided this case) that when disclosure of software is required, it is generally sufficient if the functions of the software are disclosed, it usually being the case that creation of the specific source code is within the skill of the art. *Fonar Corp. v. General Electric Co.*, Nos. 96-1075, 96-1106, and 96-1091, 1997 WL 76027, at *5 [41 USPQ2d 1801] (Fed. Cir. Feb. 25, 1997); *Hayes*, 982 F.2d at 1537-38, 25 USPQ2d at 1248-49. The functions that software program would instruct the computer to perform for controlling the machine are readily apparent from the specification of the patent at issue here, which describes the scan paths and parameters for full-tray scanning. View has not presented any evidence to controvert Robotic's assertion that one skilled in the art could generate the necessary software program to implement the disclosed functions. We therefore must conclude that the district court erred in granting summary judgment to View that the `227 patent is invalid for failure to disclose the best mode.

A recent law review article discussed the law of the Federal Circuit on the issue of computer and software patent disclosures:[81]

> n87. In recent years, the Federal Circuit has held that software patentees need not disclose source or object code, flowcharts, or detailed descriptions of the patented program. Rather, high-level functional description is sufficient to satisfy both the enablement and best mode doctrines. *See Fonar Corp. v. General Electric Co.*, 107 F.3d 1543, 1549 (Fed. Cir. 1997); *see also Graham & Zerbe*, supra note 53, at 96-97; *Mahajan*, supra note 66, at 3317. The Federal Circuit reasons that "the conversion of a complete thought ... into a language a machine understands is necessarily a mere clerical function to a skilled programmer." *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 941-42 (Fed. Cir. 1990) (quoting *In re Sherwood*, 613 F.2d 809, 817 (1980)). Indeed, the Federal

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81. Cohen, Julie et al, Patent Scope and Innovation In The Software Industry, 89 California Law Review (Jan 2001), Footnote 87.

Circuit has gone so far as to hold that patentees can satisfy the best mode requirement for inventions implemented in software even though they do not use the terms "computer" or "software" anywhere in the specification. *Robotic Vision Sys., Inc. v. View Eng'g, Inc.*, 42 U.S.P.Q.2d 1619 (Fed. Cir. 1997); *In re Dossel*, 42 U.S.P.Q.2d 1881 (Fed Cir. 1997). To be sure, in these latter cases it would probably be obvious to one skilled in the art that the particular feature in question should be implemented in software. Still, it is remarkable that the Federal Circuit is willing to find the enablement requirement satisfied by a patent specification that provides no guidance whatsoever on how the software should be written. It is simply unrealistic to think that one of ordinary skill in the programming field can necessarily reconstruct a computer program given no more than the purpose the program is to perform. The Federal Circuit's peculiar direction in the software enablement cases has effectively nullified the disclosure obligation in software cases.

1.14.6 Routine Electronic Hardware Development Does Not Involve Experimentation Even Without Considering The Actually Reduced-To-Practice "Experimental System"

All of the compelling reasons just discussed why routine software development does not involve experimentation even without considering the actually reduced-to-practice "Experimental System" **are equally applicable to routine hardware development**. This is because the same skill in the programming art also exists in the electronic hardware design art.

> "[it is a] fundamental and well understood tenet of the computing art [that] ... '**[a]ny software process can be transformed into an equivalent hardware process, and any hardware process can be transformed into an equivalent software process**.'" *See* Ed Klingler, *Microprocessor Systems Design 5* (1977). Dr. Rhyne stated that this "dualistic transformation," known as the "hardware-/software" tradeoff, effectively means that the selection of a software pointer for a microprocessor versus a hardware switch to control a microprocessor-based system is simply a matter of design choice. This record evidence shows that one of skill in the art would recognize these alternative systems as interchangeable substitutes.

Overhead Door.[82] See also Loom and Sherwood -- because electronic hardware knowledge "is common and well known [it] is as if it were written out in the patent and delineated in the drawings" and "[i]f these bridge-gapping tools are disclosed, there would seem to be no cogent reason to require disclosure of the menial tools known to all who practice this art."

It is well established that the skill in the logic design[83] art was high as of 1967:

> DeGeorge need not disclose all circuit details of a word processor or the like. DeGeorge's expert witness Tanner, a graduate electrical engineer with years of design experience on word processors, testified that "any logic designer of a normal ability should be able to implement functions given this much description [in the *per se* '670 disclosure] about them." ...
>
> It is undisputed that counters, comparison circuits, and logic circuits for detecting input signals from a word processor were all familiar to those with skill in logic design, and particularly printer control logic design, **in 1967**. **At that time,** there was nothing exotic or unique about the logic elements of the TCCPI circuit and how they interfaced with signal generating control circuits in a word processor.

DeGeorge.[84] See, e.g.; the instant disclosure at Figs. 6B-6D and 6F-6AH and Spec. at 300-371 for digital circuitry implemented with digital integrated circuits.

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82. Overhead Door v. Chamberlain, 194 F.3d 1261, 52 USPQ2d 1321, 1326 (Fed. Cir. 1999) (emphasis added).

83. "Logic design" is the design with digital "logic" (e.g.; AND gates, OR gates, NAND gates, and NOR gates) to implement digital devices (e.g.; digital processors).

84. DeGeorge v. Bernier, 768 F.2d 1318, 226 USPQ 758, 762 (Fed. Cir. 1985) (emphasis added).

1.15 The Instant Application Provides Many "Working Examples"

The presence of many "examples" in the disclosure is a very compelling fact for enablement. When this fact is considered in combination with the fact of the disclosed actually reduced-to-practice "Experimental System" and other disclosures and the fact of the predictability of the electronic and programming arts, there should be no question that the disclosure is sufficient.

The § 112-1 rejections fail to address the significant "examples" in the instant disclosure despite the fact that the CCPA established the importance of "examples" more than 40 years ago:

> In the case of alloys or mixtures .... In such cases an applicant, by fixing the ranges of proportions and describing a few **examples** throughout the range, may enable anyone skilled in the art to make any product covered by the claim, and may inform him as to what properties such a product will have.
>
> The same principle should apply to claims covering a wide range of distinct chemical compounds. However, because of the proportion of unknown compounds it will ordinarily be necessary to give **many more examples** and much more specific information than would be necessary in the case of an alloy or a mixture.

Cavallito.[85] The significant "examples" in the instant disclosure, the predictability of the electrical and programming arts, and the failure of the Examiner to properly address these important issues are very compelling reasons for reversing the § 112-1 rejections. This is even more compelling in view of the fact that, in predictable arts such as the electrical and programming arts, "examples" are not even necessary.

The Federal Circuit established that "many" examples are necessary in unpredictable arts, such as the chemical art, to support a range of compounds. Hence, the "many" examples in the instant disclosure, which is in the predictable electrical and

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85. In re Cavallito and Gray, 282 F.2d 363, 127 USPQ 202, 205 (CCPA 1960) (emphasis added).

programming arts are certainly helpful and should have been addressed with approval by the Examiner.

There should be no question that "examples" are very helpful, although not necessary, in the highly predictable electrical and programming arts. Even in the alloy and mixture arts, "by fixing the ranges of proportions and describing **a few examples** throughout the range may **enable anyone** skilled in the art **to make any product** covered by the claim":

> In the case of alloys or mixtures, however, it is generally apparent how a product of any desired proportions may be produced, and, since the properties of the aggregate ordinarily vary in accordance with the proportions of the ingredients, the characteristics of any aggregate covered by the claim can generally be **predicted** with reasonable certainty if the properties of typical aggregates are known. In such cases an applicant, **by fixing the ranges of proportions and describing a few examples throughout the range, may enable anyone skilled in the art to make any product covered by the claim, and may inform him as to what properties such a product will have**.

Cavallito.[86]

The CCPA stated with approval that Sichert sets forth "numerous examples":

> Moreover, appellant's specification sets forth numerous examples, many with exact doses and a discussion regarding the method of treatment.

Sichert.[87] Similarly, the instant disclosure also sets forth "numerous examples".

The disclosure provides various alternate embodiments (e.g.; alternate system embodiments and software and hardware embodiments) which constitute legal "examples". Just as

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86. In re Cavallito and Gray, 282 F.2d 363, 127 USPQ 202, 205 (CCPA 1960) (emphasis added).

87. In re Sichert, 566 F.2d 1154, 1164, 196 USPQ 209, 217 (CCPA 1977).

compelling, the term "example" and terms related thereto occur more than 100 times in the disclosure. The disclosed computer programs alone are "working examples".

1.15.1 The Law On Legal "Examples" Confirms The Significance Of The Actually Reduced-To-Practice "Experimental System"

The instant application provides many "working examples" and the law confirms that these "working examples" establish enablement (discussed below). A significant part of the instant disclosure provides the actually reduced-to-practice "Experimental System" in great detail.

The disclosed "examples" have significant legal weight in support of enablement. However, the § 112-1 rejections fail to provide the "substantial evidence" required by the Federal Circuit in Gartside, Kotzab, and Zurko[88] and the Examiner has failed to meet the burden imposed by the Federal Circuit in Atlas[89]:

> Use of prophetic examples, however, does not automatically make a patent non-enabling. The burden is on one challenging validity to show by clear and convincing evidence that the prophetic examples together with other parts of the specification are not enabling. Du Pont did not meet that burden here. To the contrary, the district court found that the "prophetic" examples of the specification were based on actual experiments that were slightly modified in the patent to reflect what the inventor believed to be optimum, and hence, they would be helpful in enabling someone to make the invention.

As in Atlas, the Examiner "did not meet that burden here." Even more compelling is the fact that the instant disclosure contains

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88. In re Gartside, 203 F.3d 1305, 53 USPQ2d 1769 (Fed. Cir. 2000); In re Kotzab, 217 F.3d 1365, 55 USPQ2d 1313 (Fed. Cir. 2000); and In re Zurko, 258 F.3d 1379, 59 USPQ2d 1693 (Fed. Cir. 2001).

89. Atlas Powder Co. v. E.I. Du Pont De Nemours & Co., 750 F.2d 1569, 1577, 224 USPQ 409, 414 (Fed. Cir. 1984).

hundreds of pages of "working examples" (e.g., the disclosed actually reduced-to-practice "Experimental System").

The PTO recognizes with approval "working examples", "prophetic examples", and "paper examples" and "[s]imulated or predicted test results" (MPEP 2164.02 and MPEP 608.01(p)).

> Compliance with the enablement requirement of 35 U.S.C. 112, first paragraph, does not turn on whether an example is disclosed. An example may be "working" or "prophetic." **A working example is based on work actually performed**. A prophetic example describes an embodiment of the invention based on predicted results rather than work actually conducted or results actually achieved.

MPEP 2164.02 (emphasis added). In the instant disclosure, many of the "examples" were actually performed; e.g., the actually reduced-to-practice "Experimental System" and the "examples" thereof captured on video tape (Spec. at 145-150); and other "examples" are "based on work actually performed"; e.g., "based on" the actually reduced-to-practice "Experimental System".

The PTO further discusses "examples" with approval (MPEP 608.01(p)):

> Simulated or predicted test results and prophetical examples (paper examples) are permitted in patent applications. Working examples correspond to work actually performed and may describe tests which have actually been conducted and results that were achieved. Paper examples describe the manner and process of making an embodiment of the invention which has not actually been conducted.

The Federal Circuit has approved of characterizing "prophetic examples" as equivalent to "constructive examples".

> Specifically, UC argues that a constructive or prophetic example in the `525 specification describes in sufficient detail how to prepare the claimed organism.

Regents of Univ. of Cal..[90]

The law does not require "examples" but the PTO often finds "examples" to be very significant. The PTO cites with approval to Borkowski:[91]

> However, as we have stated in a number of opinions, ... a specification need not contain a working example if the invention is otherwise disclosed in such a manner that one skilled in the art will be able to practice it without an undue amount of experimentation.

Similarly, in the instant application, "examples" are not necessary but the many "examples" that are disclosed are very compelling support for enablement. This is particularly so in view of the Borkowski invention being in the relatively unpredictable chemical art while the instant claimed invention is in the predictable electrical art and is in the high skill arts of computers and computer programs.

The disclosure itself establishes that many of the "examples" are "based upon" the disclosed actually reduced-to-practice "Experimental System". For example, the sections disclosing various "DISPLAY APPLICATIONS" (Spec. at 439-491) and the sections disclosing various "NON-DISPLAY APPLICATIONS" (Spec. at 492-502) are disclosed as being based upon the image processing system of the present invention.[92]

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90. Regents of Univ. of Cal. v. Eli Lilly & Co., 119 F.3d 1559, 43 USPQ2d 1398, 1404 (Fed. Cir. 1997).

91. In re Borkowski, 422 F.2d 904, 164 USPQ 642 (CCPA 1970) (footnote omitted) cited in MPEP 707.07(l) entitled "Comment on Examples".

92. The Table of Contents for these sections and the subsections contained thereunder are excerpted and quoted above and are further set forth in the complete Table of Contents.

1.15.2 The Disclosure Includes Many "Examples"

The instant application provides many "working examples" and the law confirms that these "working examples" establish enablement. The "working examples" are related to the disclosed actually reduced-to-practice "Experimental System". These working examples include software "working examples", hardware "working examples", and "working examples" that are combinations of hardware and software.

Many additional examples -- "prophetic examples", "paper examples", "constructive examples", and the like -- are disclosed in addition to the "working examples" in the instant application.[93] Such examples have special significance in a patent proceeding.

Because the instant application provides many "working examples" regarding the disclosed actually reduced-to-practice "Experimental System", other disclosed embodiments are enabled for the reason that their properties can readily be predicted from the "working examples". This despite the facts (a) that the electrical and programming arts are highly predictable, (b) that the other disclosed embodiments have enabling disclosures, and (c) that the other disclosed embodiments include further "examples" to supplement the "working examples":[94]

> Claims are commonly allowed for alloys or mixtures which permit **substantial variations** in the proportions of two or more ingredients. Theoretically an infinite number of products may be produced falling within the scope of such a claim. In the case of alloys or mixtures, however, **it**

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93. For convenience of discussion, the legal term "example"; such as in "working example", "prophetic example", "paper example", and "constructive example"; are shown in quotation marks while the general form of the term example, such as in -- for example -- are shown without quotation marks.

94. In re Cavallito and Gray, 282 F.2d 363, 127 USPQ 202, 204-205 (CCPA 1960) (emphasis added).

> **is generally apparent how a product of any desired proportions may be produced**, and, since the properties of the aggregate ordinarily vary in accordance with the proportions of the ingredients, the characteristics of any aggregate covered by the claim can generally be **predicted** with reasonable certainty if the properties of typical aggregates are known. In such cases an applicant, **by fixing the ranges of proportions and describing a few examples throughout the range, may enable anyone skilled in the art to make any product covered by the claim, and may inform him as to what properties such a product will have**.

Because "a few examples" enable **ranges** of products in the alloy and mixture arts, certainly the extensive disclosure and specific "examples" (not just "ranges") enable the instant claim limitations. This is even more compelling because the electrical and programming arts are even more predictable than the alloy and mixture arts.

The Table of Contents and the sections listed provide many "examples" of display and non-display applications.

TABLE OF CONTENTS

* * *

Table of Contents.

The video tapes of operation of the disclosed actually reduced-to-practice "Experimental System" and the discussions related thereto in the disclosure (Spec. at 145-150, "Experimental System Video Tape") provide many additional "working examples".

The disclosure itself establishes that many of the "examples" are "based upon" the disclosed actually reduced-to-practice "Experimental System". For example, the sections disclosing various "DISPLAY APPLICATIONS" (Spec. at 439-491) and the sections disclosing various "NON-DISPLAY APPLICATIONS" (Spec. at 492-502) are disclosed as being "based upon" the image processing system of the present invention.[95]

> DISPLAY APPLICATIONS
>
> General
>
> Display applications for **the image processing disclosed herein** are many and varied. Most display applications currently satisfied with CG and CIG systems can use **the present image processing system of the present invention** ....
>
> Most display applications needing image processing capability can use **the present image processing system of the present invention.** These image processing applications include medical image processing, video special effects, and many others....
>
> **The system of the present invention** can be used for training of personnel, such as a simulator; as a display for a vehicle, such as for an aircraft cockpit display; for investigation and evaluation of large dynamic range database information, such as with LANDSAT images; and for many other applications.

Spec. at 439-440 (first two emphases in original, all other emphasis added).

> NON-DISPLAY APPLICATIONS
>
> General Description
>
> Various applications of **the system of the present application** are non-display applications; such as automatic pattern recognition, robotics, and artificial intelligence applications.

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95. The Table of Contents for these sections and the subsections contained thereunder are excerpted and quoted above and are further set forth in the complete Table of Contents.

Spec. at 492-493 (first two emphasis in original, all other emphasis added).

1.16 The Issues In Ex Parte Richards Compel A Similar Reversal Of The § 112-1 Rejection Based Upon Disclosure Of "Interconnections" And Failure Of The Examiner To Establish A Prima Facie Case

The Board in Richards[96] found that an apparently sparse disclosure of "standard components" and the failure of the Examiner to establish a prima facie case warranted reversal of an enablement rejection. These issues are very similar to the issues in the instant appeal, interconnections the failure of the Examiner to establish a prima facie case. While the appellant in Richards merely relies on parts of three pages of disclosure for an example, the present Applicant, in significant contrast thereto, relies on more than two hundred pages of detailed disclosure of an actually reduced-to-practice "Experimental System" embodiment and much more. Further, the appellant in Richards failed to argue a prima facie case issue, yet the Board therein still held that "the examiner has not met his burden" (Richards at 4). In significant contrast thereto, the present Applicant argued the failure of the Examiner to establish a prima facie case.

The issues of "interconnections" and the Examiner's failure to establish a prima facie case should be treated in the instant application in the same manner that the Board treated these issues in Richards at 3-4:

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96. Ex parte Richards, Appeal No. 1999-1847 (Bd. Pat. App. & Int.) (unpublished opinion), *at* http://www.uspto.gov/web/offices/dcom/bpai/decisions/fd991847.pdf. See also U.S. Patent No. 6,382,101 (issued May 7, 2002 to Richards).

OPINION ...

> The examiner maintains that the structural connections, circuitry and cooperation are not sufficiently disclosed.... We find that the examiner has not attempted to establish why the supporting specification in combination with the relevant prior art fails to enable the claims which is the examiner's initial burden. **In re Marzocchi**, 439 F.2d 220, 223, 169 USPQ 367, 369 (CCPA 1971). From our review of the examiner['s] rejection, the examiner maintains that the programming and specific interconnection of the functional units "must" be disclosed in the specification.... We disagree with the examiner. The examiner provides no reasoned analysis of why these would be needed or required.... The examiner carries the initial burden to establish a case. Here, the examiner has not met his burden, and we will not sustain the rejection of claims 7-12 under 35 U.S.C. § 112, first paragraph.
>
> However, appellant has not argued that the examiner failed to establish a ***prima facie*** case, but merely that the specification is enabling to those skilled in the art. ...

It is worth repeating (Richards at 3-4):

> From our review of the examiner['s] rejection, the examiner maintains that the programming and specific interconnection of the functional units "must" be disclosed in the specification.... We disagree with the examiner. The examiner provides no reasoned analysis of why these would be needed or required.

If "the programming and specific interconnection of the functional units" need not be disclosed in Richards, then it seems inconsistent to maintain the § 112-1 rejection in the instant application which has extensive disclosure of "programming and specific interconnection of the functional units". As in Richards, the instant claimed invention makes use of such "standard components which are connected by standard electrical connections".

In Richards, the Board found that "a basic example of the operation of the invention" on parts of three pages of the specification was sufficient (Richards at 4):

> However, appellant has not argued that the examiner failed to establish a ***prima facie*** case, but merely that the specification is enabling to those skilled in the art. ... Furthermore, appellant relies on a basic example of the operation of the invention at pages 5 and 6 of the brief. Appellant cites to only specific portions of pages 5, 6, and 7 of the specification to support the example.

If this was sufficient to support a finding in Richards that the specification is enabling, then certainly the instant disclosure with more than **30 figures** (e.g., Figs. 6A-6AH) and more than **200 pages** of very detailed written disclosure **specifically directed to the disclosed actually reduced-to-practice "Experimental System" embodiment** (in addition to extensive additional disclosure) must be sufficient.

The instant disclosed actually reduced-to-practice "Experimental System" embodiment with its extensive use of "standard components which are connected by standard electrical connections" (e.g., commercially available products) must certainly be sufficient in view of the Board's finding in Richards that "standard components ... connected by standard electrical connections" are sufficient (Richards at 4):

> Appellant argues that the devices in the specification and claims are standard components which are connected by standard electrical connections and that one skilled in the art would be able to make and use the invention without undue experimentation. ... We agree with appellant.

In view of the Board's holding in Richards, the instant disclosed actually reduced-to-practice "Experimental System" embodiment having significantly greater disclosure than the applied references must certainly be sufficient. In Richards, the Board reached its decision regarding the sufficiency of Richards' disclosure by noting that the Wuhrl reference "contains a similar level of description as the instant description with respect to the interconnection of standard elements and does not

provide any of the specifics for programming these standard functional units" (Richards at 4-5):

> Specifically, the prior art to Wuhrl applied against the claims is indicative of the level of skill in the relevant art. Wuhrl contains a similar level of description as the instant description with respect to the interconnection of standard elements and does not provide any of the specifics for programming these standard functional units. Similarly, we find that from the basic functional description of these standard components, it would have been obvious to one of ordinary skill in the art at the time of the invention to program and interface these components together to make and use the system to aid in the selection of ink fountains for adjustment by an operator.

Just as in Richards, the applied references in the instant application have much less disclosure than the instant application but are still presumed to be sufficiently disclosed.

In Richards, the Board commented that it would have been obvious for an artisan to program and interface the standard components "from the basic functional description of these standard components" (Richards at 5):

> Similarly, we find that from the basic functional description of these standard components, it would have been obvious to one of ordinary skill in the art at the time of the invention to **program and interface** these components together to make and use the system to aid in the selection of ink fountains for adjustment by an operator.

However, the instant application discloses far more than a "basic functional description of ... standard components". It discloses commercially available operating system software and source code for custom computer programs (discussed herein) and it discloses commercially available computer **interface** boards (e.g., two Compupro Interfacer-II board and one Compupro System Support board. See Spec. at 297 (emphasis added):

> The computer is implemented with various S-100 boards manufactured by CompuPro including the 8085-8088 CPU board, RAM 16 and RAM 17 memory boards, **a System Support board**, and **a pair of Interfacer 2 boards**. One Interfacer 2 board is used **to interface to the terminal and printers**.

> The other Interfacer 2 board provides **the 3-channel parallel interface** to the control logic. These boards are described in detail in the referenced manuals.

And this disclosure is in the highly predictable electronics art where one skilled in the art would know how to program and interface standard components. This notwithstanding the fact that the instant application has extensive programming and interfacing disclosure.

II. TRAVERSE OF 37 CFR 1.83 AND 37 CFR 1.75 OBJECTIONS

The Applicant traverses the 37 CFR 1.75 objection and the 37 CFR 1.83 objection (the "'75 objection" and "'83 objection") for the reasons of record.

The objections fail to establish a non-prima facia case for the reasons of record and for the reasons set forth below.

The '75 and '83 objections do not establish a prima facie case. For example, the subject features are shown and are recited at numerous places in the extensive disclosure, but the objections completely disregard the extensive disclosure and instead makes general statements about the absence of the subject features in the disclosure.

The '75 and '83 objections are improper constructive rejections of claims and are in conflict with the 35 USC 112-1 rejection. For example, this issue is covered by the 35 USC 112-1 rejection in the instant action and this issue is clearly appealable; hence this issue cannot also be covered by an objection which is petitionable.

It is well established that it is the content and not the form of the disclosure that is important In re Sherwood, 204 USPQ 537, 545 footnote 8 (CCPA 1980). The claim elements are shown in the figures sufficient to meet 37 CFR 1.83(a). A requirement for any more would violate In re Sherwood.

The Examiner's conclusory statements objecting to the drawings are not evidence and certainly not the required "substantial evidence" (see below). However, the drawings themselves constitute "substantial evidence", are presumed to be correct,[97] and satisfy § 112-1 and the PTO requirements regarding drawings. Hence, clarification is requested regarding the particular claim limitations that the Examiner contends are

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97. See MPEP 2164.04. See also In re Marzocchi, 439 F.2d 220, 169 USPQ 367 (CCPA 1967).

missing from the drawings and reasons why the drawings as filed do not illustrate such claim limitations.

35 USC § 113 establishes that a drawing isn't even necessary ("The applicant shall furnish a drawing **where necessary**.... **When** the nature of such subject matter admits of illustration by a drawing ...." (emphasis added)).

37 CFR § 1.83(a) establishes that a labeled box is suitable ("conventional features disclosed in the description ... should be illustrated in the drawing in the form of a graphical drawing symbol or a labeled representation (e.g., a labeled rectangular box)").

The objection mischaracterizes the issue. There is nothing in the drawings that is objectionable, it is the recitations in the claims that the Examiner finds objectionable. The Examiner cannot object to the drawings for what is not shown in the drawings, there is nothing inherently wrong with the drawings by themselves. The Examiner is actually objecting to the claims as not having a basis in the drawings. However, this issue must involve a rejection. Without a rejection involving the drawings, the Examiner cannot make an objection to the drawings. This is because "[the Board's] decision regarding the § 112 rejection governs the merits of the objection". The objection based on the language of the claims cannot stand alone without a rejection. See Ex parte Kazmierczak,[98] at 5.

The Federal Circuit requires "substantial evidence" to support a rejection. See Gartside and Kotzab.[99]

> The reviewing court shall --
>
> * * *
>
> (2) hold unlawful and set aside agency actions, findings, and conclusions found to be --

---

98. Ex parte Kazmierczak, Appeal No. 97-3469 (Bd. Pat. App. & Int.) (unpublished opinion), at http://www.uspto.gov/web/offices/dcom/bpai/decisions/fd973469.pdf. See also U.S. Patent No. 6,005,751 (issued December 21, 1999 to Kazmierczak).

99. In re Gartside, 53 USPQ2d 1769 (Fed. Cir. 2000); In re Kotzab, 55 USPQ2d 1313 (Fed. Cir. 2000).

* * *

(E) unsupported by substantial evidence ....

Gartside.[100]

The Applicant further traverses the 37 CFR 1.75 objection and the 37 CFR 1.83 objection for the reasons shown in Section I herein. For example, the 37 CFR 1.83 objection addresses the showing of the claimed invention in the figures, which is addressed in Sections 1.2 and 1.8 herein). For example, Fig. 1A is an end-to-end block diagram, from the input end at the left to the output end at the right with processing, storing, and other functions therebetween.

As discussed in Section 1.2 above:

> A system block diagram is shown in Figs 1A and 1P with various blocks that are shown in greater detail in other figures. For example, many of the blocks shown in Fig. 1A are expanded to provide greater detail in Figs. 1C-1G and in the "Modular Configuration Features Table" (Spec. at 24-30). Effectively, the more detailed block diagrams in Figs. 1C-1G are intended to fit within the corresponding blocks in Fig. 1A and the more detailed functions in the "Modular Configuration Features Table" are intended to fit within the corresponding blocks in Fig. 1A (Spec. at 5, 17, 17; respectively (emphasis added):
>
> > ... where **Fig 1A** is a block diagram representation of one configuration of the system of the present invention; Fig 1B is a block diagram of a geometric module configuration; **Fig 1C** is a block diagram of a single channel configuration of one configuration of the present invention **in accordance with a reduced implementation of Fig 1A**; **Fig 1D** is a block diagram of a geometric processor module **in accordance with Fig 1A**; **Fig 1E** is a block diagram of a spatial processor module **in accordance with Fig 1A**; **Fig 1F** is a block diagram of input sources, input interfaces, and input multiplexers/demultiplexers **in accordance with Fig 1A**; Fig 1G is a block diagram of an output interface, output multiplexers/demultiplexers, and output devices **in accordance with Fig 1A**; ....

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100. In re Gartside, 53 USPQ2d 1769, 1773 (Fed. Cir. 2000).

The block diagram shown in **Fig 1A** illustrates the modular expandability of the system of the present invention, **shown in greater detail in Figs 1B to 1G**.

One general purpose modular configuration is shown in **Figs 1A to 1G** and **summarized in the MODULAR CONFIGURATION FEATURES TABLE herein**.

Particularly note that the disclosure in Figs. 1C-1G and in the "Modular Configuration Features Table" (Spec. at 24-30) are expressly disclosed as being part of Fig. 1A. Also, particularly note the discussion of the self-contained embodiment in Section 1.2 herein.

III. THE EXAMINER HAS FAILED TO PROVIDE THE REQUIRED "SUBSTANTIAL EVIDENCE" AND HAS FAILED TO ESTABLISH A PRIMA FACIE CASE TO COUNTER THE APPELLANT'S ENTITLEMENT TO A PATENT

The Applicant is entitled to a patent. The Examiner is required to provide "substantial evidence" and to establish a prima facie case in order to challenge the Applicant's entitlement thereto. However, the Examiner has not provided the required "substantial evidence" and has not established a prima facie case. Instead, the Examiner relies on unsupported conclusory statements and on irrelevant statements. Such statements are expressly discouraged by the Federal Circuit and do not satisfy the requirement for providing "substantial evidence".

3.1 The Applicant Is Entitled To A Patent

The Applicant is entitled to a patent because he has met the legal requirements. The Examiner not provided the "substantial evidence" and has not established a prima facie case to challenge this entitlement.

Judge Plager, in his concurring opinion in Oetiker[101], stated:

> An applicant for a patent is entitled to the patent unless the application fails to meet the requirements established by law. It is the Commissioner's duty (acting through the examining officials) to determine that all requirements of the Patent Act are met. The burden is on the Commissioner to establish that the applicant is not entitled under the law to a patent. In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967), cert. denied, 389 U.S. 1057 (1968). In rejecting an application, factual determinations by the PTO must be based on a preponderance

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101. In re Oetiker, 977 F.2d 1443, 1449, 24 USPQ2d 1443, 1447 (Fed. Cir. 1992).

> of the evidence, and legal conclusions must be correct. In [sic] re Caveney, 761 F.2d 671, 674, 226 USPQ 1, 3 (Fed. Cir. 1985).
>
> The process of patent examination is an interactive one. See generally, Chisum, Patents, § 11.03 et seq. (1992). The examiner cannot sit mum, leaving the applicant to shoot arrows into the dark hoping to somehow hit a secret objection harbored by the examiner. The 'prima facie case' notion, the exact origin of which appears obscure (see In re Piasecki, 745 F.2d 1468, 1472, 233 USPQ 785, 788 (Fed. Cir. 1984)), seemingly was intended to leave no doubt among examiners that they must state clearly and specifically any objections (the prima facie case) to patentability, and give the applicant fair opportunity to meet those objections with evidence and argument. To that extent the concept serves to level the playing field and reduces the likelihood of administrative arbitrariness. * * *
>
> Specifically, when obviousness is at issue, the examiner has the burden of persuasion and therefore the initial burden of production. Satisfying the burden of production, and thus initially the burden of persuasion, constitutes the so-called prima facie showing. Once that burden is met, the applicant has the burden of production to demonstrate that the examiner's preliminary determination is not correct. The examiner, and if later involved, the Board, retain the ultimate burden of persuasion on the issue.
>
> If, as a matter of law, the issue is in equipoise, the applicant is entitled to the patent. Thus on appeal to this court as in the PTO, the applicant does not bear the ultimate burden of persuasion on the issue. In the end there is no reason there or here to argue over whether a 'prima facie' case was made out. The only determinative issue is whether the record as a whole supports the legal conclusion that the invention would have been obvious.

Similarly, in the instant case, the Examiner has not met his burden with factual determinations, based on a preponderance of the evidence, or with proper legal conclusions. Hence, the Applicant is entitled to a patent as a matter of law.

3.2 The U.S. Supreme Court And The Federal Circuit Require "Substantial Evidence" To Support A Rejection

The Federal Circuit requires "substantial evidence" to support a rejection. See Gartside and Kotzab.[102]

> The reviewing court shall --
>
> * * *
>
> (2) hold unlawful and set aside agency actions, findings, and conclusions found to be --
>
> * * *
>
> (E) unsupported by substantial evidence ....

Gartside.[103]

"[W]e review the Board's underlying factual findings for substantial evidence ...." Kotzab.[104]

In this case, the rejections are not supported by "substantial evidence", but rather are supported by irrelevant and erroneous arguments and improper conclusory statements. Hence, the rejections cannot stand.

"Substantial evidence" is described by the Federal Circuit as follows:

> [T]he "substantial evidence" standard asks whether a reasonable fact finder could have arrived at the agency's decision.

Gartside.[105] The Gartside court quotes the U.S. Supreme Court in Consolidated[106]:

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102. In re Gartside, 53 USPQ2d 1769 (Fed. Cir. 2000); In re Kotzab, 55 USPQ2d 1313 (Fed. Cir. 2000).

103. In re Gartside, 53 USPQ2d 1769, 1773 (Fed. Cir. 2000).

104. In re Kotzab, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 2000).

105. In re Gartside, 53 USPQ2d 1769, 1773 (Fed. Cir. 2000) (citing Consolidated Edison Co. v. NLRB, 305 U.S. 197, 229 (1938)).

106. In re Gartside, 53 USPQ2d 1769, 1773 (Fed. Cir. 2000) (quoting Consolidated Edison Co. v. NLRB, 305 U.S. 197, 229-30 (1938)) (parenthetical added, ellipsis in original).

> It ["substantial evidence"] means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion .... Mere uncorroborated hearsay or rumor does not constitute substantial evidence.

But the rejections are not supported by "substantial evidence". Instead, the Examiner relies on conclusory statements and irrelevant and erroneous statements. Hence, the rejections violate the law of the Federal Circuit and the law of the U.S. Supreme Court.

3.3 The Examiner Relies On Conclusory Statements And Irrelevant Statements, Which Are Expressly Discouraged By The U.S. Supreme Court And By The Federal Circuit

The Examiner relies on conclusory statements and irrelevant statements, which are expressly discouraged by the U.S. Supreme Court and by the Federal Circuit. The Gartside court quotes the U.S. Supreme Court in Consolidated[107]:

> It ["substantial evidence"] means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion .... Mere uncorroborated hearsay or rumor does not constitute substantial evidence.

This is confirmed in Kotzab.[108]

> Whether the Board relies on an express or an implicit showing, it must provide particular findings related thereto .... Broad conclusory statements standing alone are not "evidence."

However, the rejections are not supported by "substantial

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107. In re Gartside, 53 USPQ2d 1769, 1773 (Fed. Cir. 2000) (quoting Consolidated Edison Co. v. NLRB, 305 U.S. 197, 229-30 (1938)) (parenthetical added, ellipsis in original).

108. In re Kotzab, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

evidence". Instead, the Examiner relies on conclusory statements and irrelevant and erroneous statements.

The Federal Circuit requires the PTO to "explicate its factual conclusions", but the Examiner provides irrelevant arguments and conclusory arguments.

> We have expressly held that the Board's opinion must explicate its factual conclusions, enabling us to verify readily whether those conclusions are indeed supported by "substantial evidence" contained within the record. See Gechter v. Davidson, 116 F.3d 1454, 1460, 43 USPQ2d 1030, 1035 (Fed. Cir. 1997)

Gartside.[109]

> Whether the Board relies on an express or an implicit showing, it must provide particular findings related thereto .... Broad conclusory statements standing alone are not "evidence."

Kotzab.[110]

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109. In re Gartside, 53 USPQ2d 1769, 1774 (Fed. Cir. 2000).

110. In re Kotzab, 55 USPQ2d 1313 (Fed. Cir. 2000).

IV. ART REJECTIONS

4.1 35 USC 103 Rejections

The Applicant respectfully traverses the 35 USC 103 rejections for the reasons of record and for the additional reasons below.

The 35 USC 103 rejections fail to establish a non-prima facia case for the reasons of record and for the reasons set forth below.

The § 103 rejections do not properly address the nature of the references nor the combinations of the references. For example, the rejections do not establish why such references are pertinent to the instant claimed invention. Further, the references are directed to different types of systems with different types of implementations therebetween where the manner of making the combinations is not obvious.

> Tescher is directed to transform domain coding for compression.
>
> Tiemann is directed to a video block system.
>
> Jain is directed to estimating block displacement.

Merely finding disconnected bits-and-pieces in the prior art is insufficient.

The Examiner has not properly established how such diverse references can be combined. See Amgen, Inc. v. Chugai Pharmaceutical Co., Ltd., 927 F.2d 1200, 18 USPQ2d 1016 (Fed. Cir. 1991).

> When the patented invention is made by combining known components to achieve a new system, the prior art must provide a suggestion or motivation to make such a combination. Heidelberger Druckmaschinen AG v. Hantscho Commercial Products Inc., 21 F.3d 1068, 30 USPQ2d 1377 (Fed. Cir. 1994).

In an appeal in an ancestor application Hyatt `355,[111] Judge Barrett clarified the requirement for motivation:

> [T]hat a fact may be well known ... does not itself provide the motivation for the combination.

The art rejections herein are similar to the art rejections in the appeal in this Hyatt '355 application[112] where the art rejections were all reversed.

As in the instant case, the examiner in Hyatt-'355 relied on improper hindsight to support § 103 rejections. Thus, the Board reversed all of the § 103 rejections in Hyatt-'355:

> The examiner fails to show a suggestion of the limitations in the prior art. "Obviousness may not be suggested using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (citing W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1551, 1553, 220 USPQ 303, 311, 312-13 (Fed. Cir. 1983)). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992) (citing In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991)). "'[T]he question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, 974 F.2d 1309, 1311-12, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992) (quoting Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed. Cir. 1984)).
>
> * * *
>
> Although Hobrough teaches "automatic registration of photographic images," col. 3, ll. 49-50, the examiner fails to identify a sufficient suggestion to add the automatic registration of Hobrough to the system of Hemstreet. There is no evidence that the sample and the patterns to be

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111. Ex parte Hyatt, Appeal No. 1994-3042, Paper No. 39 at 36 in patent application Serial No. 07/289,355 (PTO Bd. App. December 21, 2000) [herein Hyatt-`355] (unpublished PTO decision).

112. Ex parte Hyatt, Appeal No. 1994-3042, Paper No. 39 in patent application Serial No. 07/289,355 (PTO Bd. App. December 21, 2000) [herein Hyatt-`355] (unpublished PTO decision).

compared in Hemstreet are misregistered so as to benefit from registration.

* * *

... the examiner fails to allege, let alone show, that the reference cures the deficiency of Hemstreet and Hobrough.

Hyatt-'355 at 27-29.

4.2 35 USC 102 Rejections

The Applicant respectfully traverses the 35 USC 102 rejections for the reasons of record and for the additional reasons below.

The 35 USC 102 rejections fail to establish a non-prima facia case for the reasons of record and for the reasons set forth below.

The references relied on for the § 102 rejections do not provide the identicality necessary to support the § 102 rejections.

The 35 USC 102 rejection does not establish a prima facie case. For example, the Federal Circuit **requires** that a '102 rejection must be supported on a limitation by limitation basis with specific fact findings for each contested limitation and satisfactory explanations for such findings. Claim construction must also be explicit. Gechter v. Davidson, 43 USPQ2d 1031 at 1035.

Further, under 35 USC 102, every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. In re Bond, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990) as cited in Gechter v. Davidson, 43 USPQ2d 1031 at 1032.

The law requires **identity** between the rejected claims and the references for a 35 USC 102 rejection; as discussed below. However, the rejection does not establish this identity. This is not surprising, there is no such identity. The claims have features that distinguish over the references.

A party asserting that a patent claim is anticipated under 35 USC 102 must demonstrate, among other things, identity of invention. Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 771, 218 USPQ 781, 789 (Fed. Cir. 1983), cert. denied, 465 U.S. 1026 [224 USPQ 520] (1984), overruled in part on another ground, SRI Int'l v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1125, 227 USPQ 577, 588-89 (Fed. Cir. 1985) (in banc). Identity of invention is a question of fact, and one who seeks such a finding must show that each element of the claim in issue is found, either expressly or under principles of inherency, in a single prior art reference, or that the claimed invention was previously known or embodied in a single prior art device or practice. Minnesota Mining and Manufacturing v. Johnson & Johnson, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992)

Rejection for anticipation or lack of novelty requires, as the first step in the inquiry, that all the elements of the claimed invention be described in a single reference. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir.), cert. denied, 110 S.Ct. 154 (1989). Further, the reference must describe the applicant's claimed invention sufficiently to have placed a person of ordinary skill in the field of the invention in possession of it. In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990)

An anticipation analysis must be conducted on a limitation by limitation basis, with specific fact findings for each contested limitation and satisfactory explanations for such findings. Claim construction must also be explicit. Anticipation requires that every limitation in the claim was identically shown in a single reference. Gechter v. Davidson, 116 F.3d 1454, 43 USPQ2d 1031 at 1035 (Fed. Cir. 1997)

The Examiner alleges correspondence between claimed elements and elements shown in the reference. However, allegations of correspondence between claimed elements is no substitute for a proper showing of identity.

The rejection relies on bits and pieces found in the prior art. However, the finding of bits and pieces of the claimed

invention does not establish anticipation.

> "Only god works from nothing. Man must work with old elements." (65 J.Pat.Off.Soc'y 331; Howard T. Markey; Chief Judge; Court of Appeals for the Federal Circuit).

Just because the elements existed does not mean that they are combined in the claimed manner or that they cooperate in the claimed manner.

Other case law further illustrates the deficiencies in the 35 USC 102 rejection.

> Anticipation under 35 U.S.C.A. paragraph 102 can be found only when reference discloses exactly what is claimed. Titanium Metals Corp. of America v. Banner, 778 F.2d 775. (C.A. Fed. DC 1985).

> "7. The prior art relied on by plaintiff does not constitute an anticipation of claims 18, 19 and 20 of the Wollard patent under 35 U.S.C. paragraph 102. Anticipation can exist only where a single prior art reference teaches the same elements as claimed, united in the same way to perform an identical function. Illinois Tool Works, Inc. v. Sweetheart Plastics, Inc., 436 F.2d 1180, 168 USPQ 451 (7th Cir. 1971); McCullough Tool Co. v. Wells Survey, Inc., 343 F.2d 381, 398, 145 USPQ 6, 19-20 (10th Cir. 1965); cert. denied 383 U.S. 933, 148 USPQ 772 (1966)." Penn Yan Boats, Inc. v. Sea Lark Boats, Inc., 175 USPQ 260, 273 (S.D.Fla 1972).

The Federal Circuit has established that the party asserting anticipation (in the present case, the patent examiner) demonstrate the identity between the claimed invention and the reference by showing that each element of the claim was either expressly or inherently described in a single prior art reference or that the claimed invention was known previously or encompassed in a single prior art device or practice. See Kalman v. Kimberly-Clark Corp., 713 F.2d 771, 218 USPQ 789 (Fed.Cir 1983). The Federal Circuit confirmed this standard of anticipation in In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed.Cir. 1985) and Ralston Purina Co. v. Far-Mar-Co, Inc., 772 F.2d 1570, 1574, 227 USPQ 177, 180 (Fed.Cir. 1985).

The references relied on for the § 102 rejections do not provide the identicality necessary to support the § 102 rejections.

Jain is directed to estimating block displacement.

Tescher is directed to transform domain coding for compression.

The 35 USC 102 rejection does not establish a prima facie case. For example, the Federal Circuit **requires** that a '102 rejection must be supported on a limitation by limitation basis with specific fact findings for each contested limitation and satisfactory explanations for such findings. Claim construction must also be explicit. Gechter v. Davidson, 43 USPQ2d 1031 at 1035.

Further, under 35 USC 102, every limitation of a claim must identically appear in a single prior art reference for it to anticipate the claim. In re Bond, 910 F.2d 831, 832, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990) as cited in Gechter v. Davidson, 43 USPQ2d 1031 at 1032.

The law requires **identity** between the rejected claims and the references for a 35 USC 102 rejection; as discussed below. However, the rejection does not establish this identity. This is not surprising, there is no such identity. The claims have features that distinguish over the references.

V. COMMENTS ON AMENDMENTS TO THE CLAIMS

The amendments to the claims are proposed in order to more particularly point out the Applicant's invention, in order to impart precision, and in order to more fully protect the invention described in the disclosure of the instant application.

VI. AMENDMENTS

Please amend the claims as set forth in Appendix A attached hereto.

CERTIFICATION OF MAILING BY EXPRESS MAIL: I hereby certify that this correspondence is being deposited with the United States Postal Service with Express Mail post office to addressee service under 37 CFR 1.10, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 with the express mail label number EV 323876261 on November 3, 2004.

Respectfully submitted,

Dated: November 3, 2004

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